

MODEL NAME : *Astro2*  
PCB NO : *LA-A271*  
BOM P/N : *xxxx*

# Compal Confidential

## Schematics Document

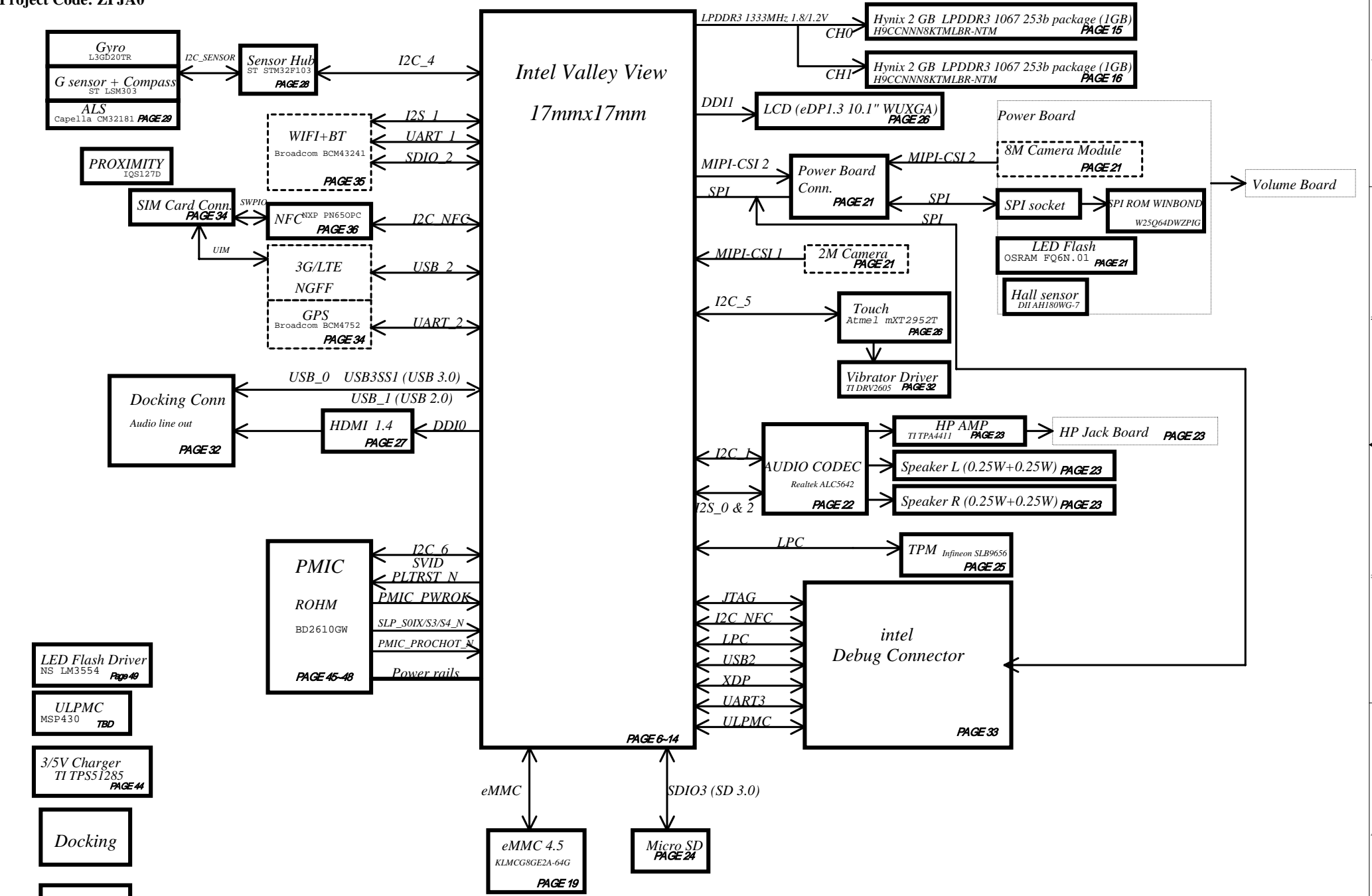
Intel Bay Trail

2013-07-17

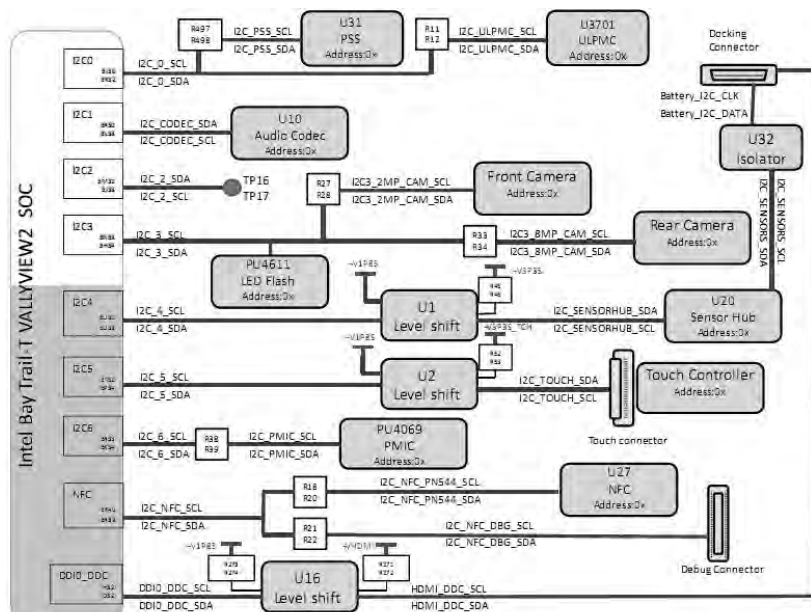
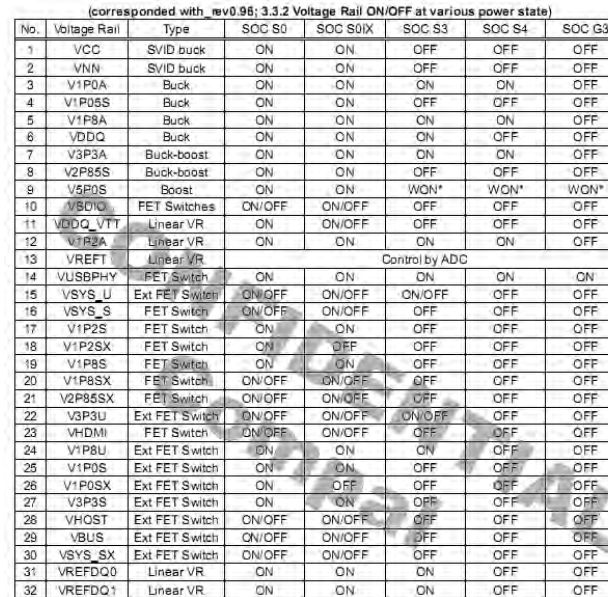
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Astro2 Block Diagram





S4/S5 to S0 (Power Up) Sequence      Cold Boot Sequence Diagram



4G@ : For 4G LPDDR3 SKU config

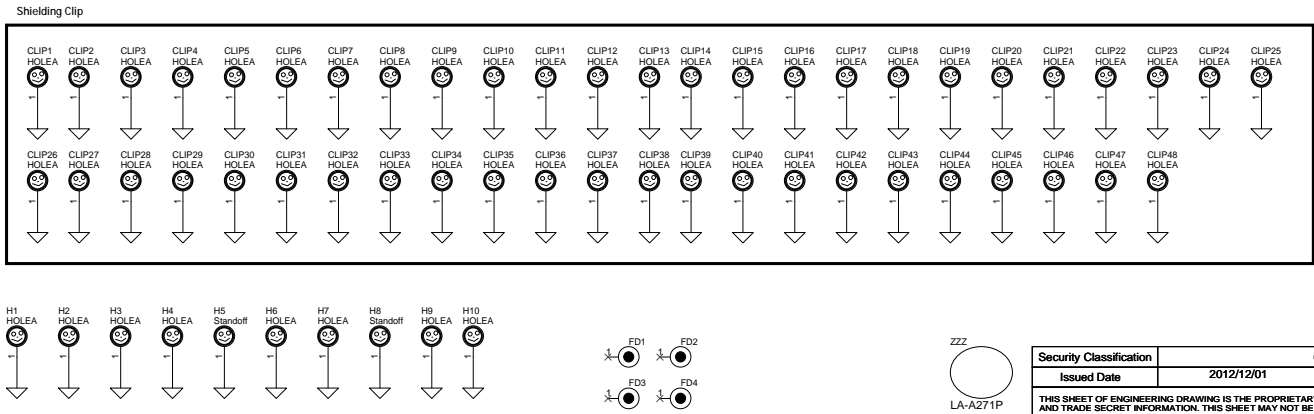
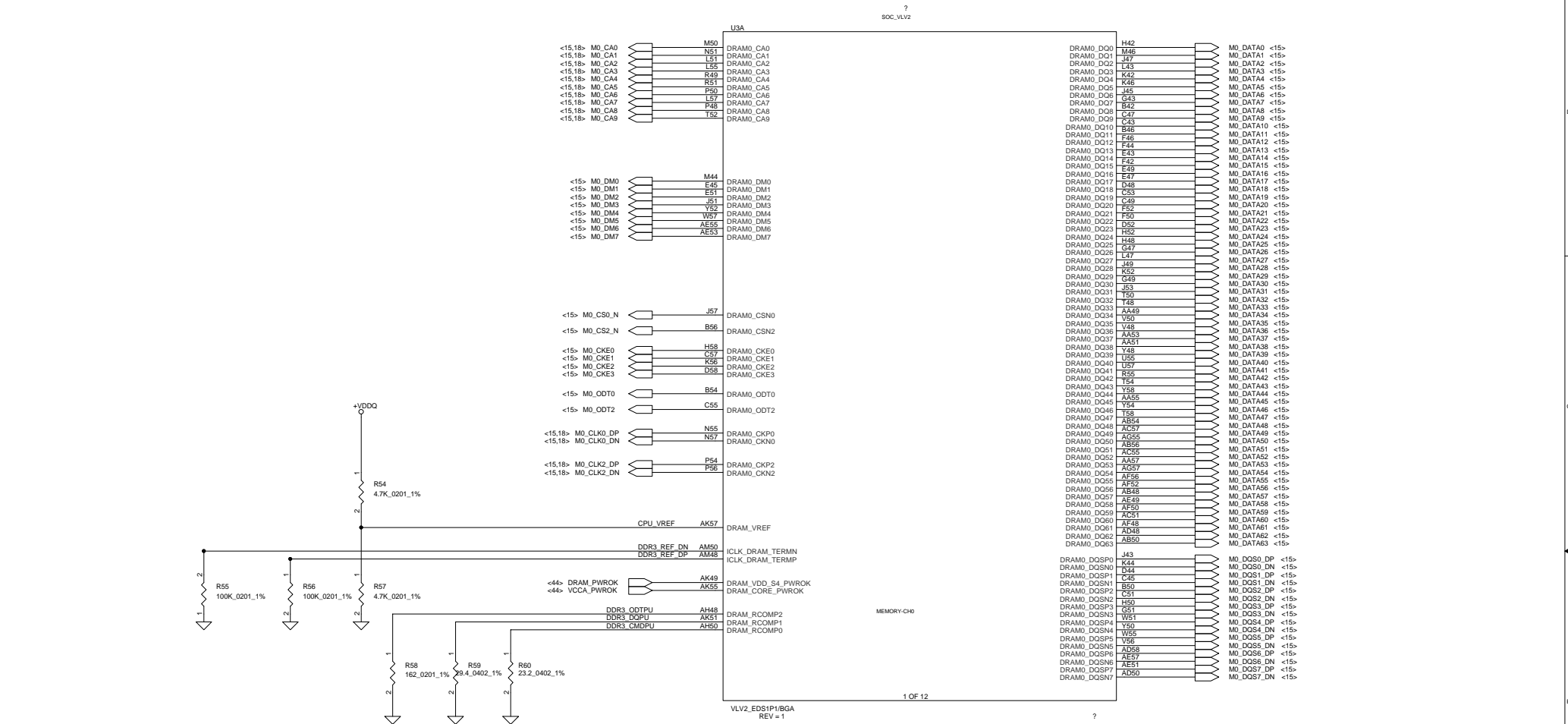
**Symbol Note :**

 : means Digital Ground

 : means Analog Ground

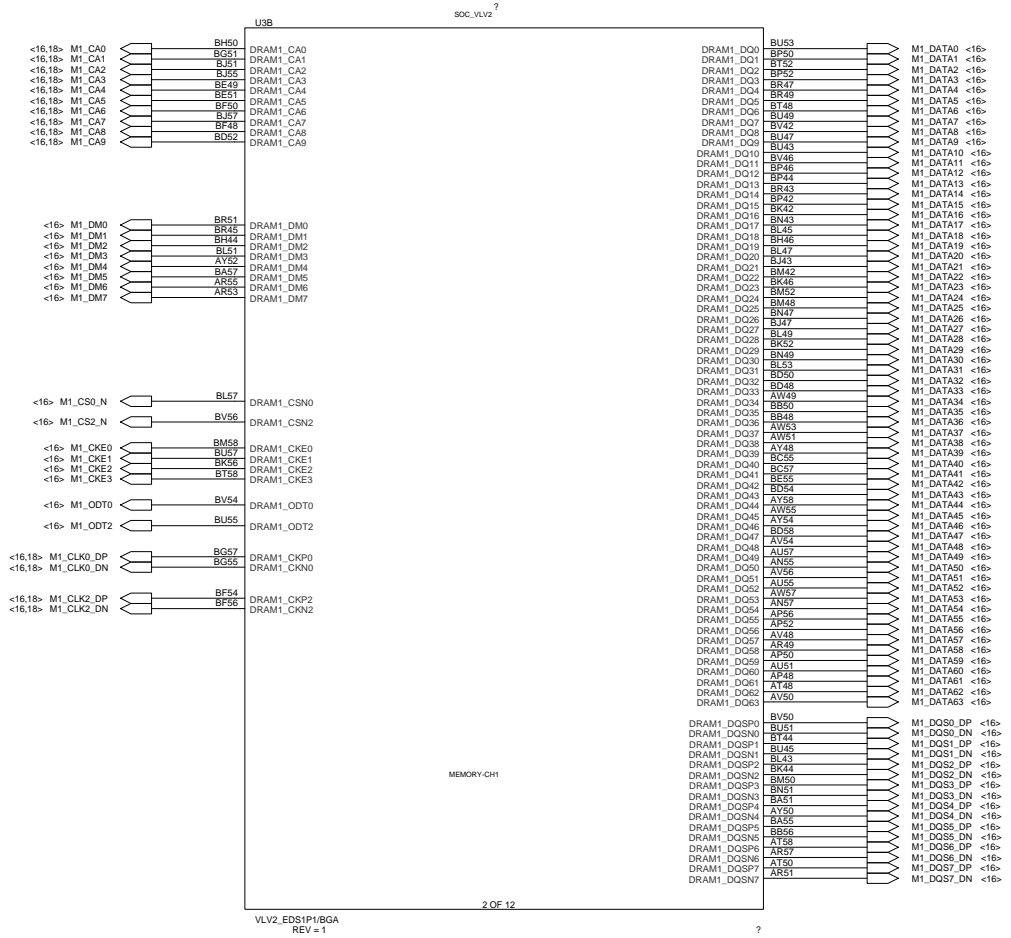
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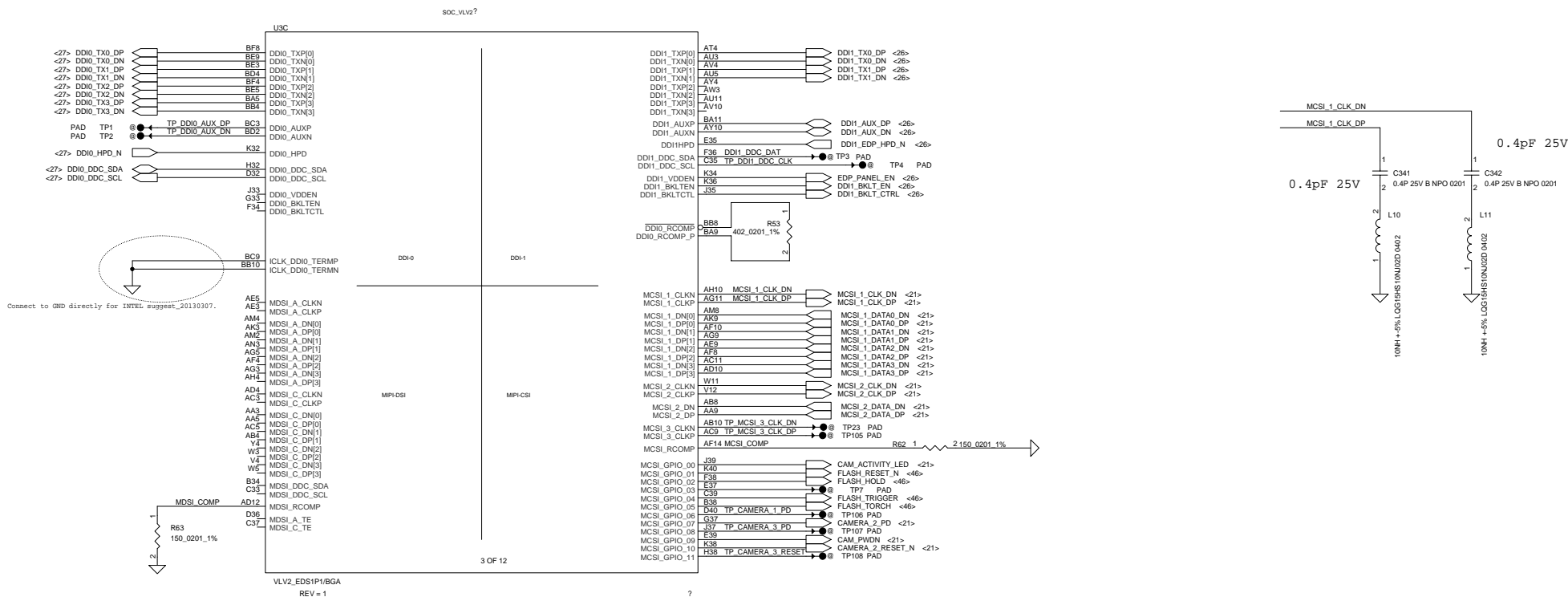


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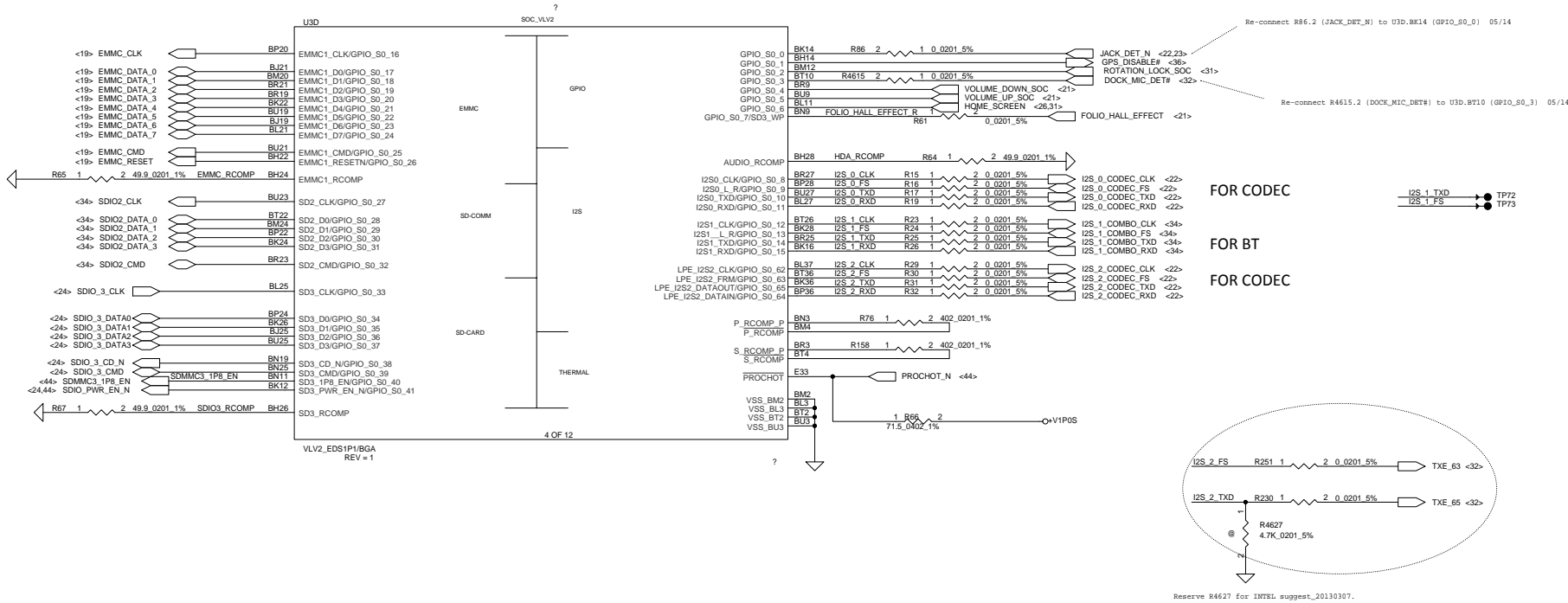


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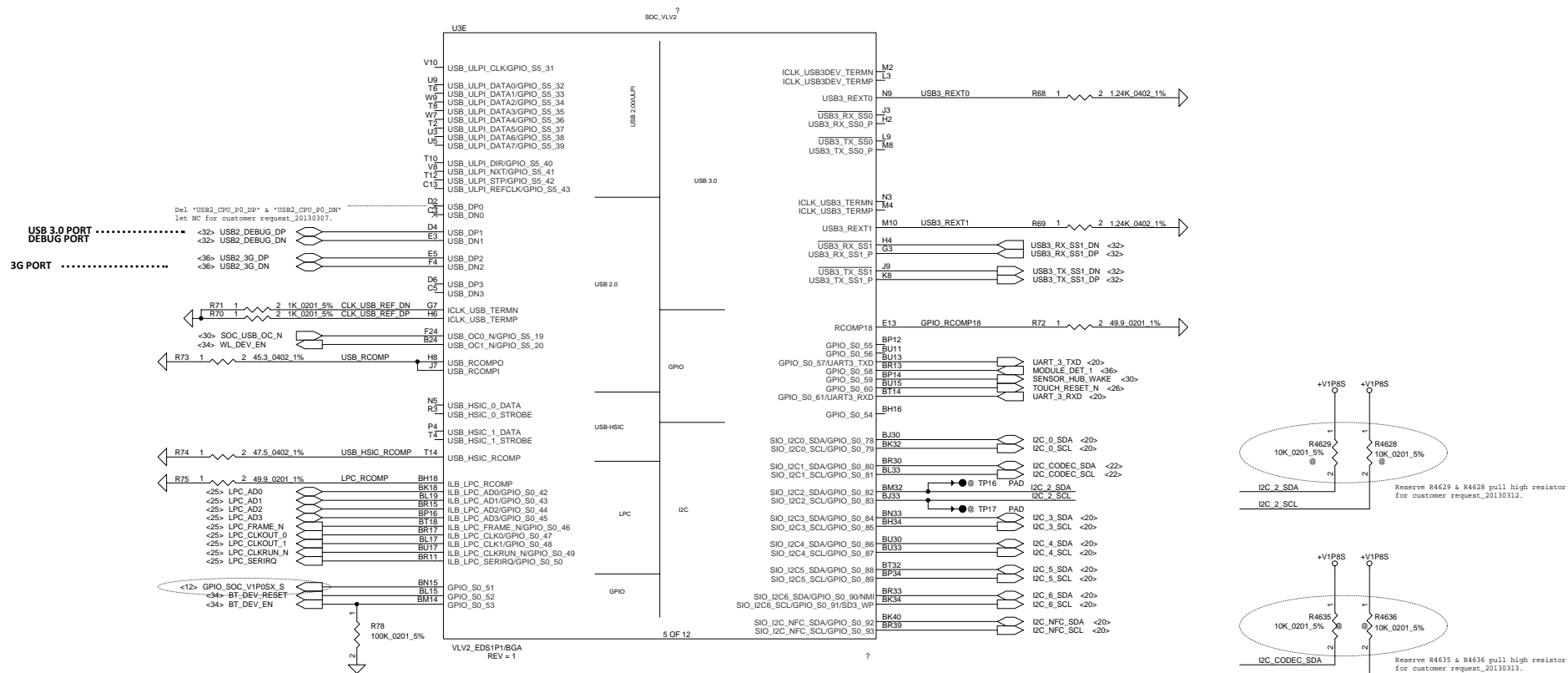


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SOC:STORAGE AND AUDIO



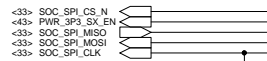
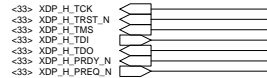
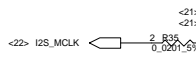
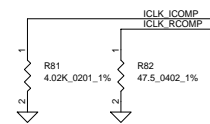
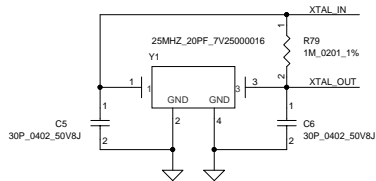
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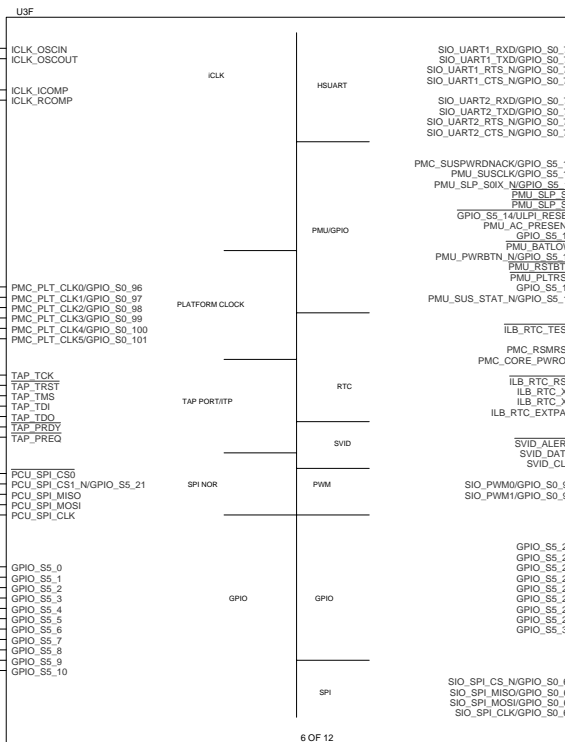
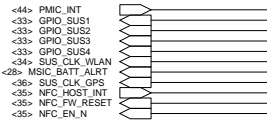
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# SOC:CLOCK,DEBUG & MISC



## RF Request

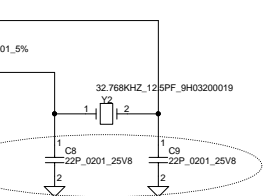
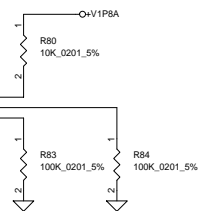


VLV2\_EDS1P1/BGA

REV = 1

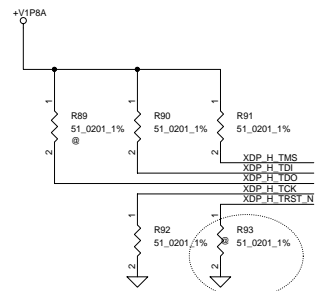
Connect DOCK\_HP\_DET#\_R to Soc GPIO\_55\_14

Change NGPF\_RESET to control GPS\_POWER\_ON 05/14



USM\_DETECT\_SOC R52 2 1 0.0201.5%

WWAN\_WAKE\_N\_SOC R87 1 2 0.0201.5%



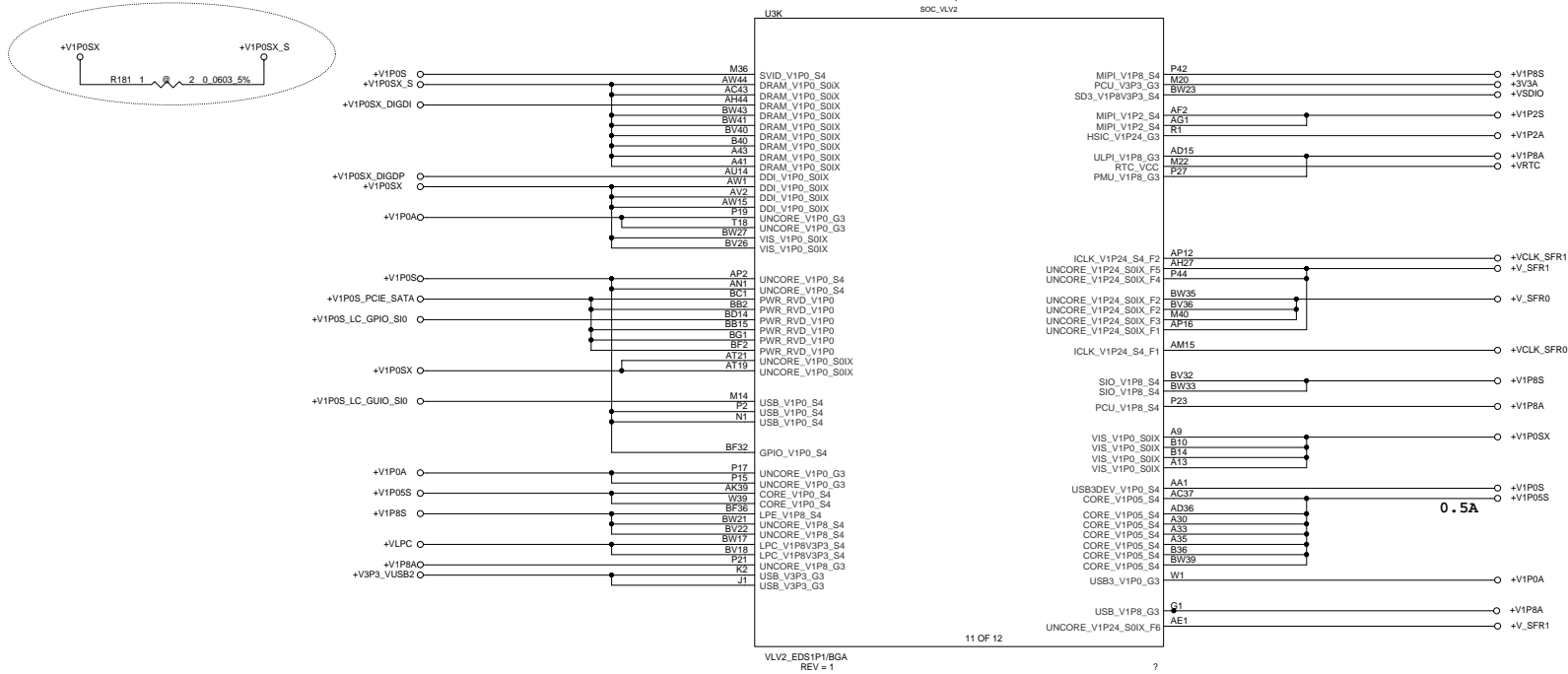
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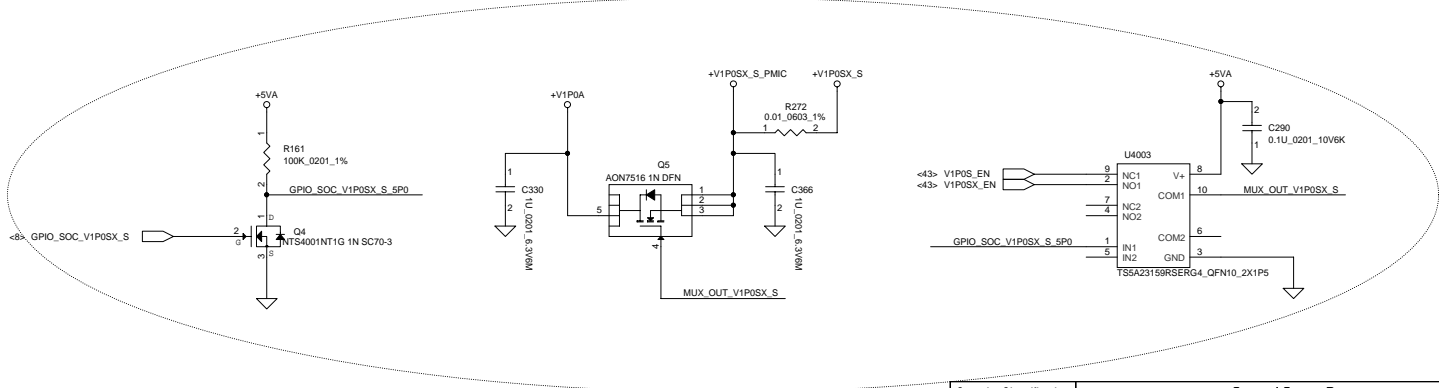


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SOC: POWER

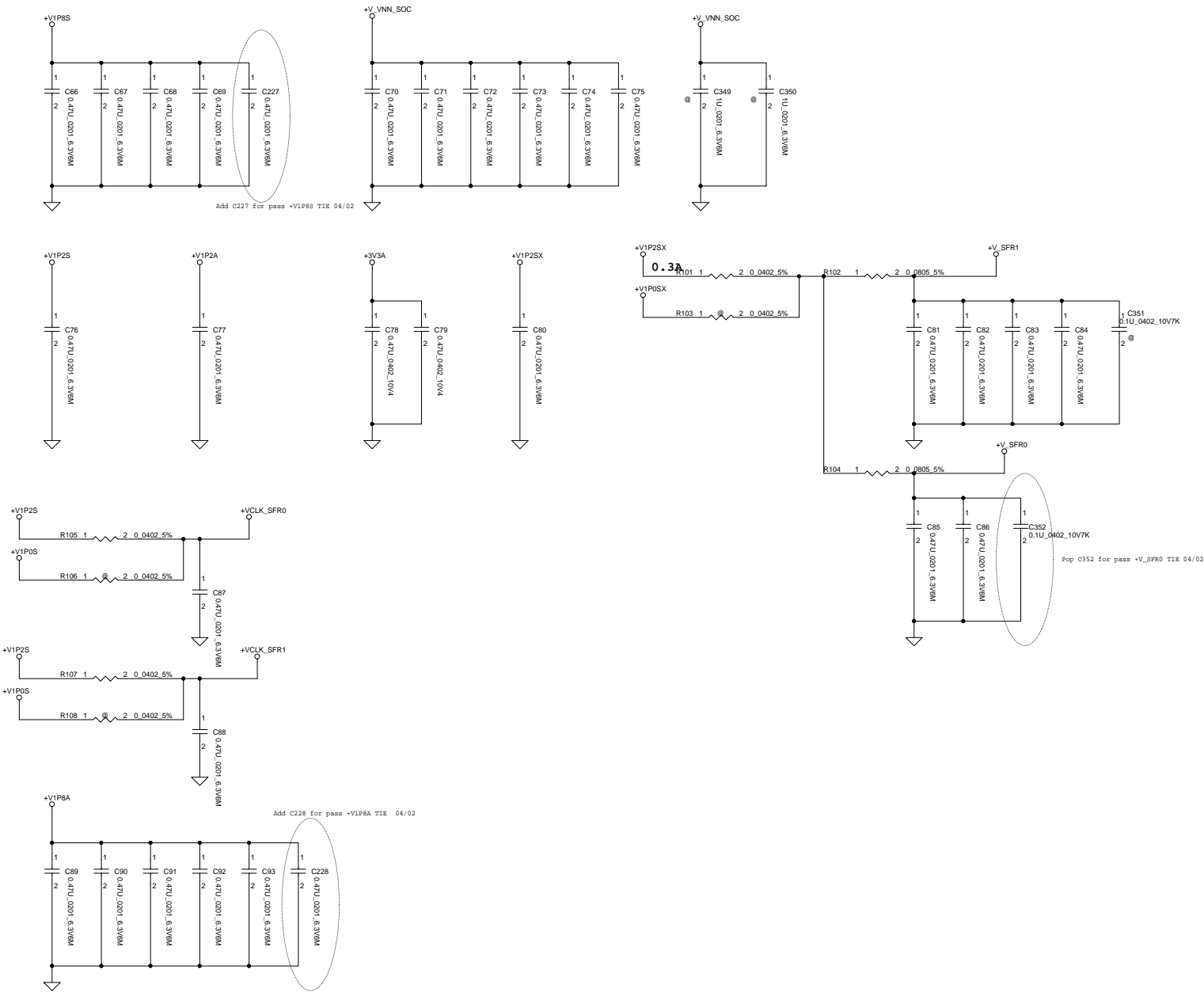


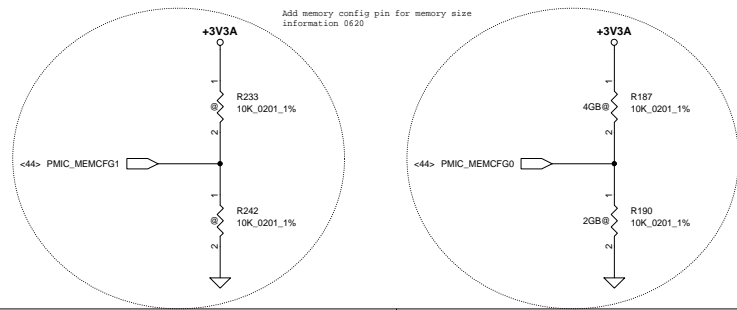
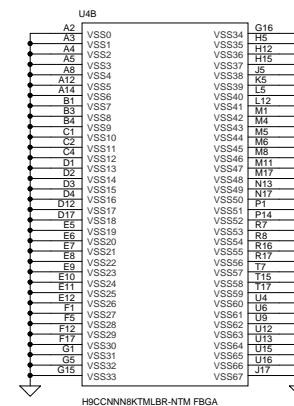
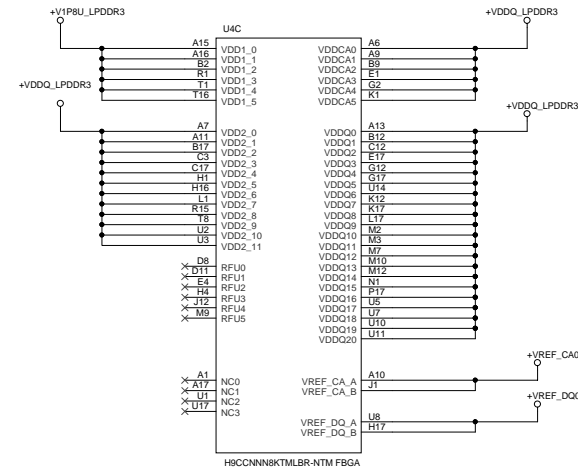
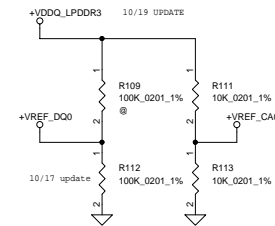
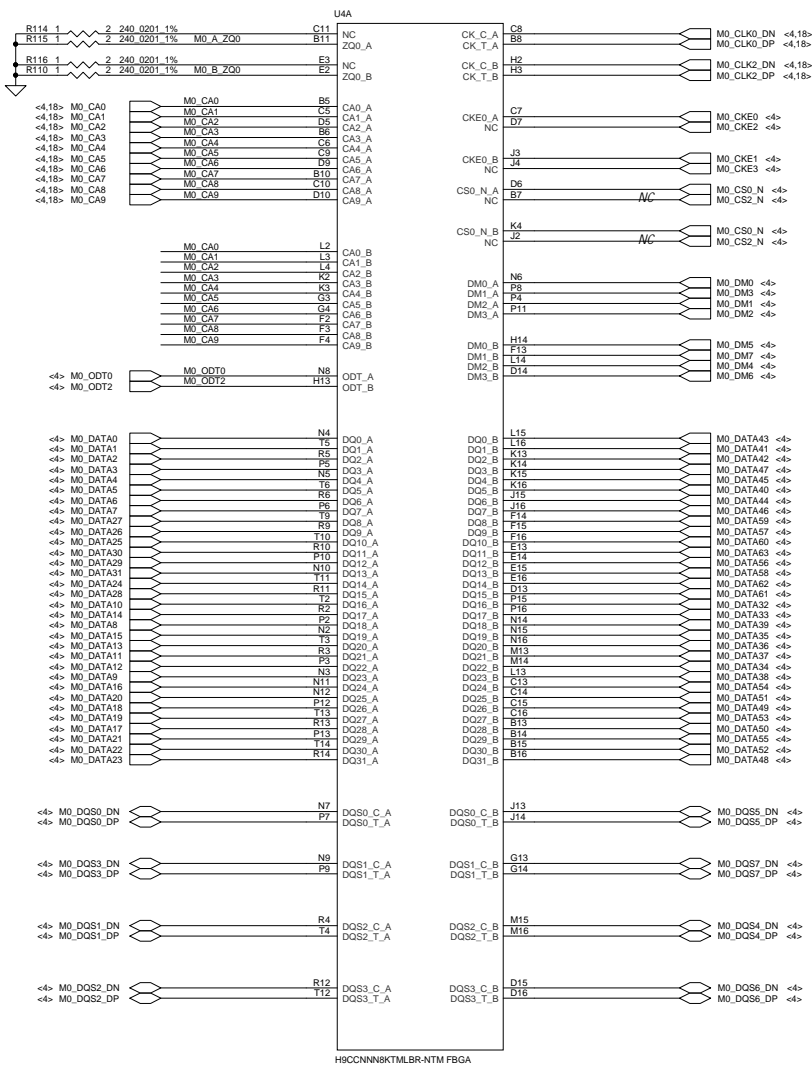
Add the multiplexer circuit for DDRIO power rail control 05/02



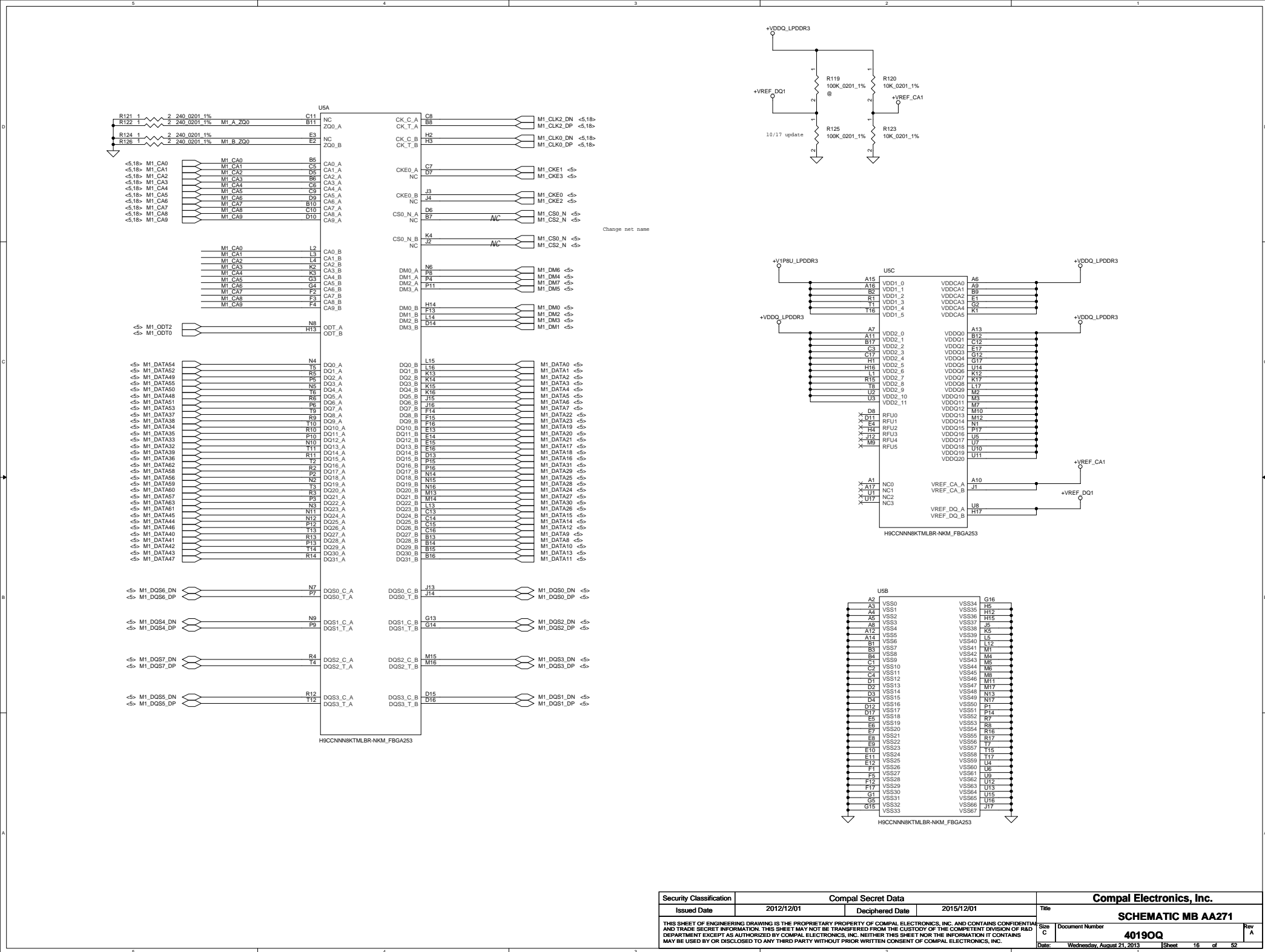


SOC DECOUPLING

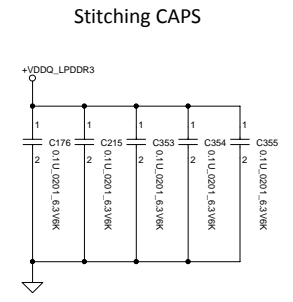
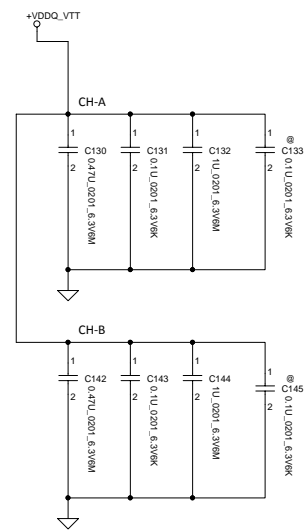
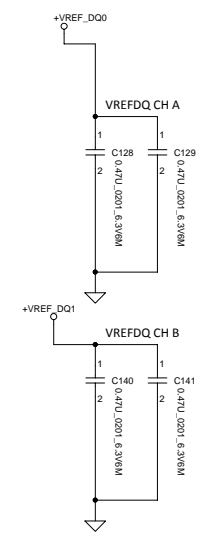
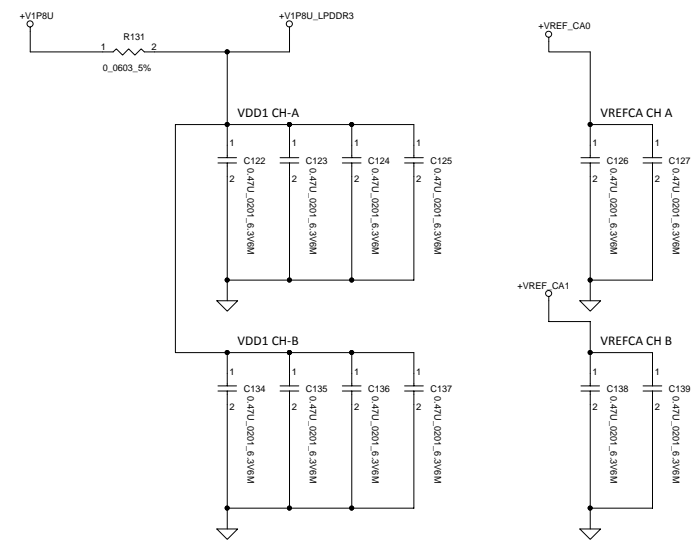
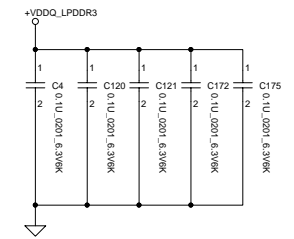
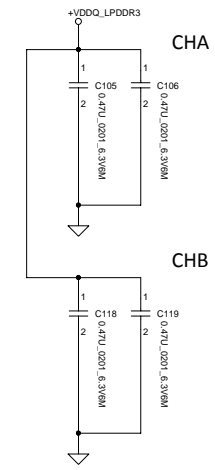
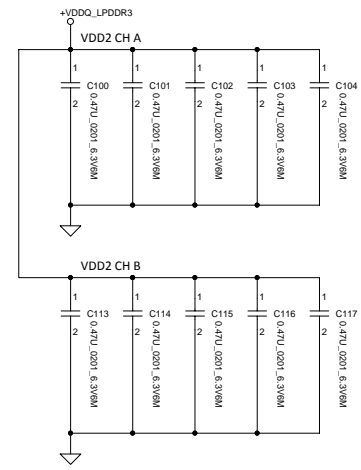
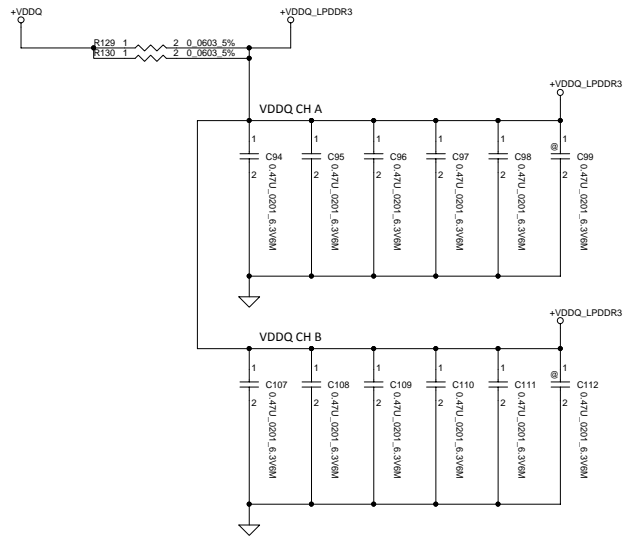


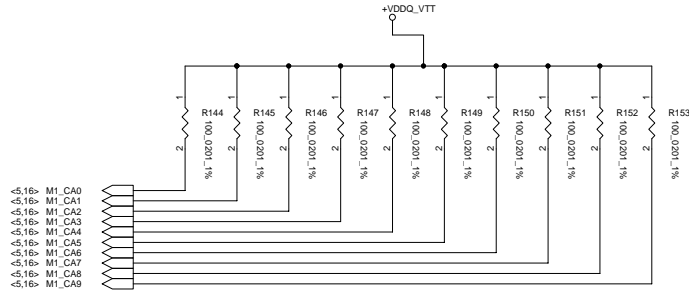
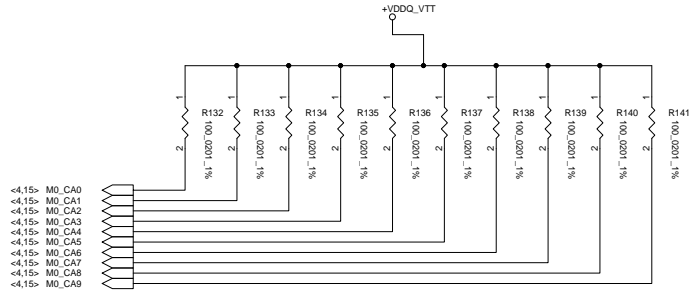
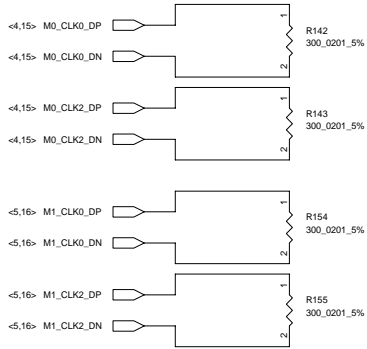


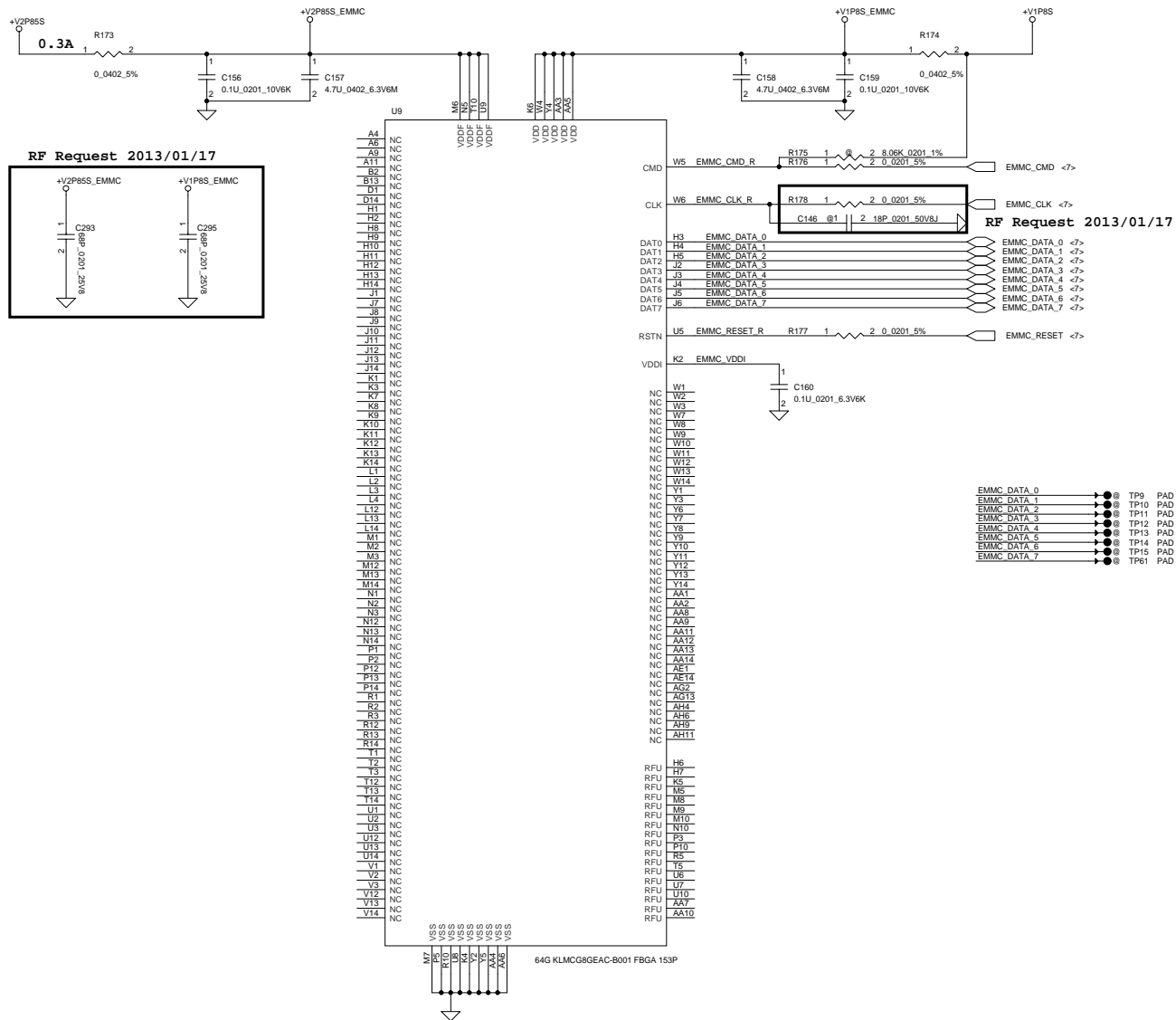
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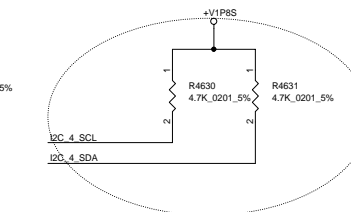
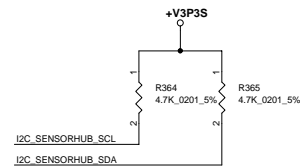
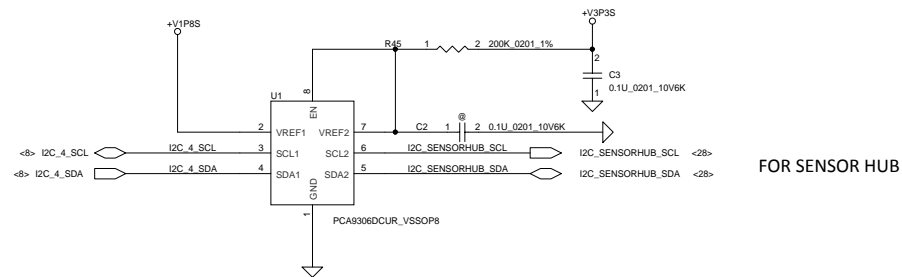
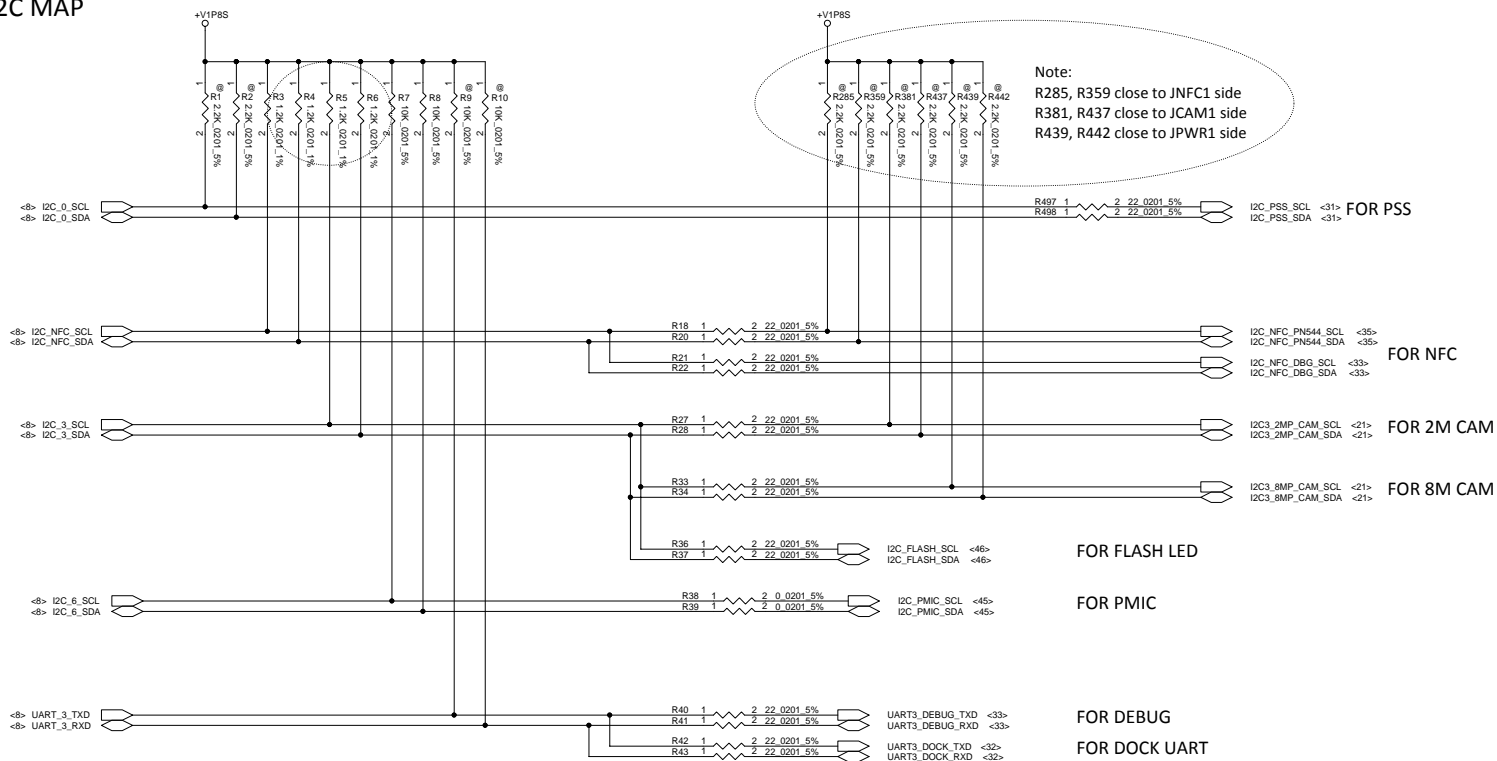




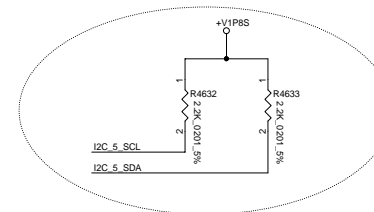
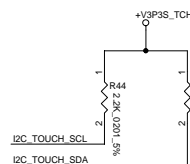
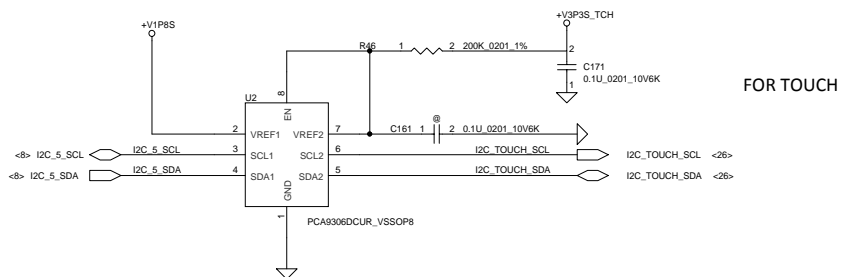




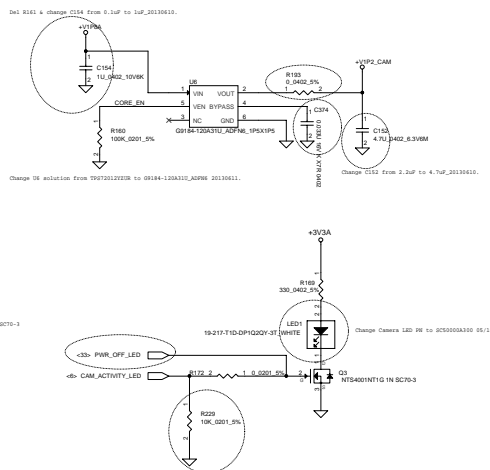
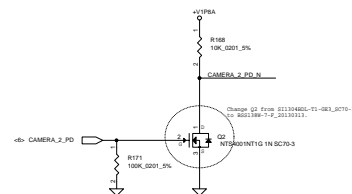
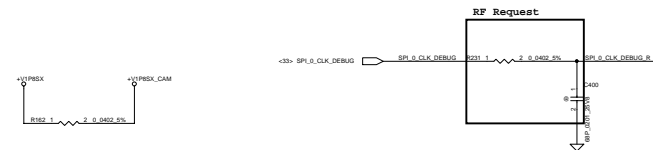
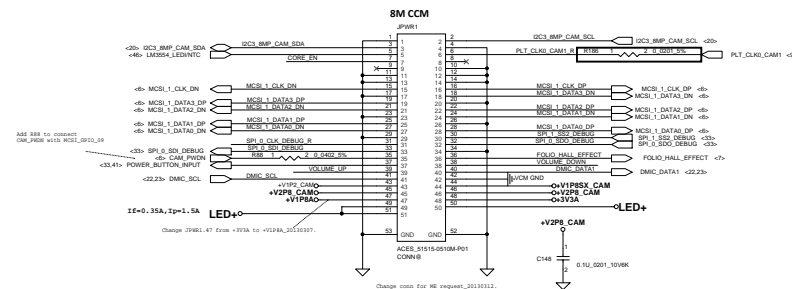
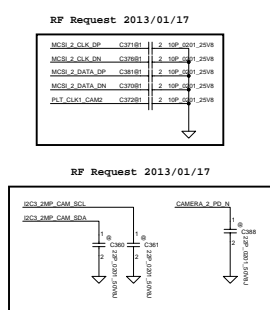
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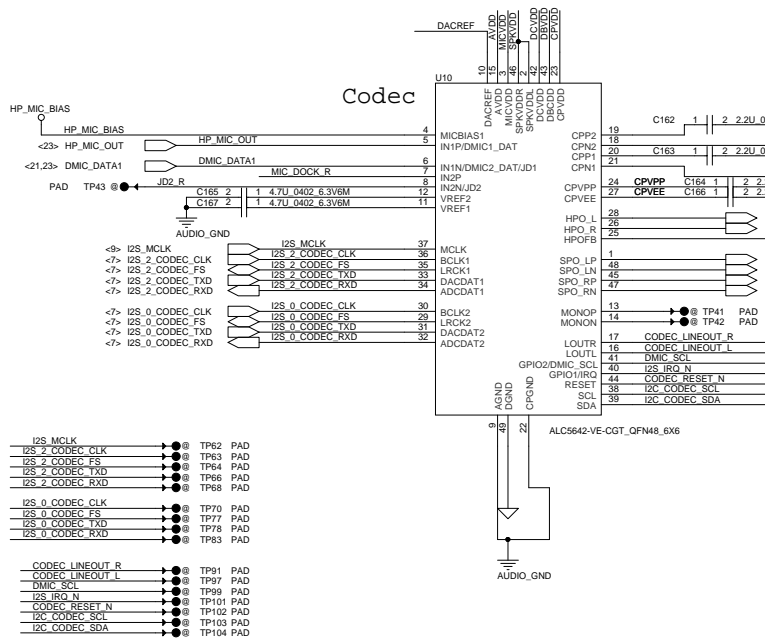
Add R4630 & R4631; R4632 & R4633 pull high resistor for customer request\_20130312.



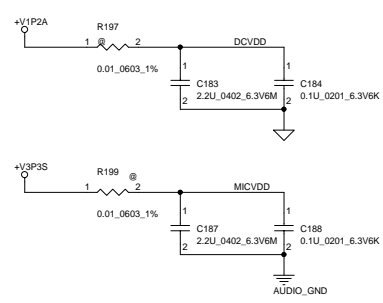
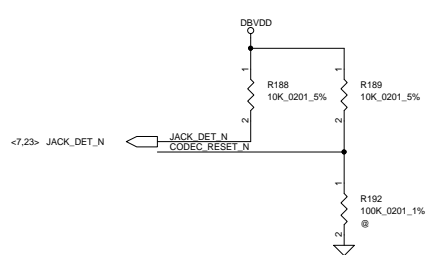
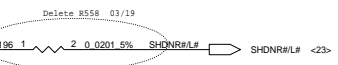
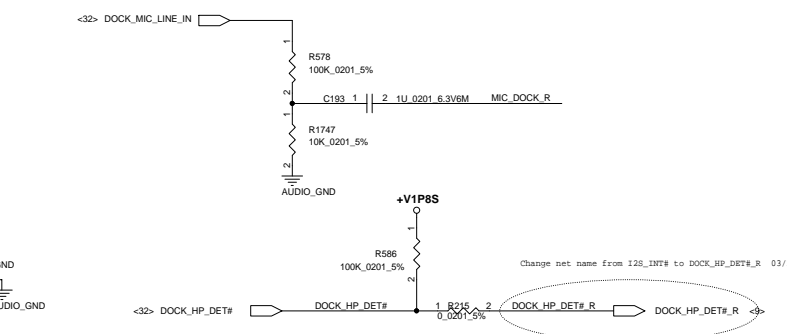
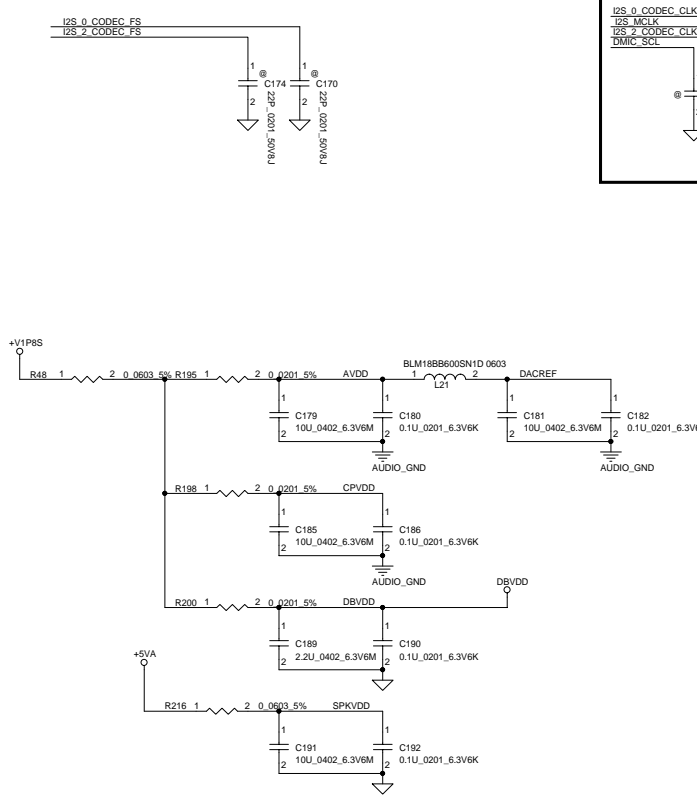
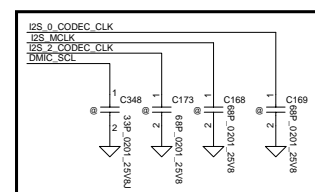
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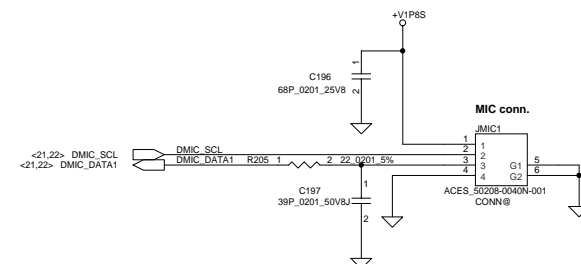
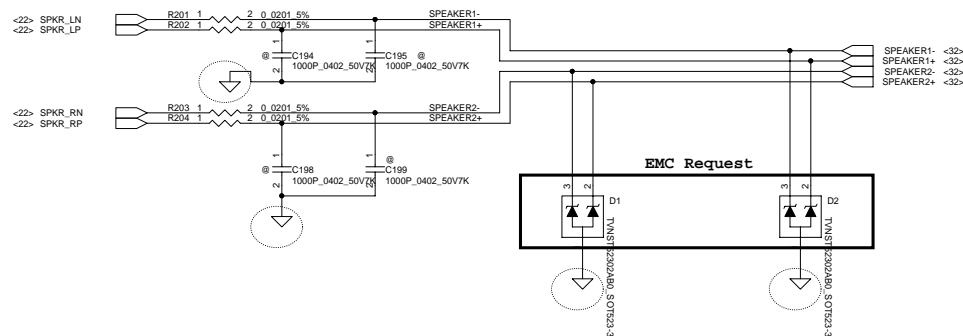


RF Request 2013/01/17

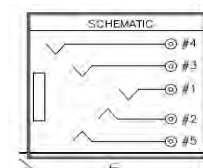
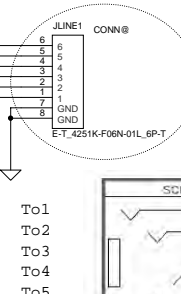
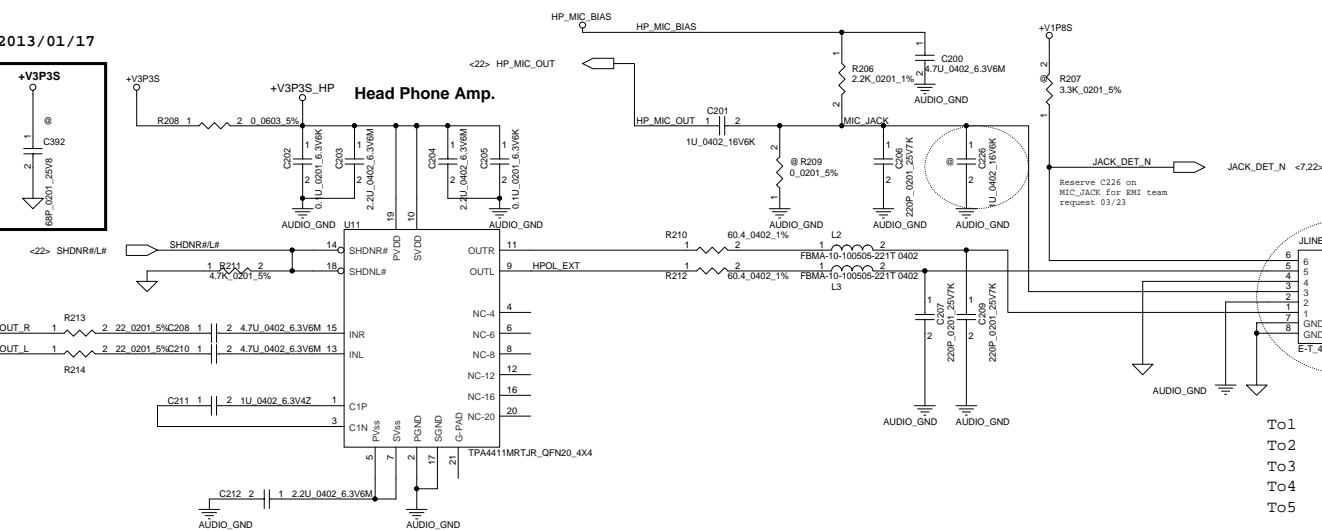
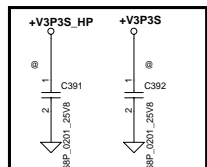


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## SPEAKERS



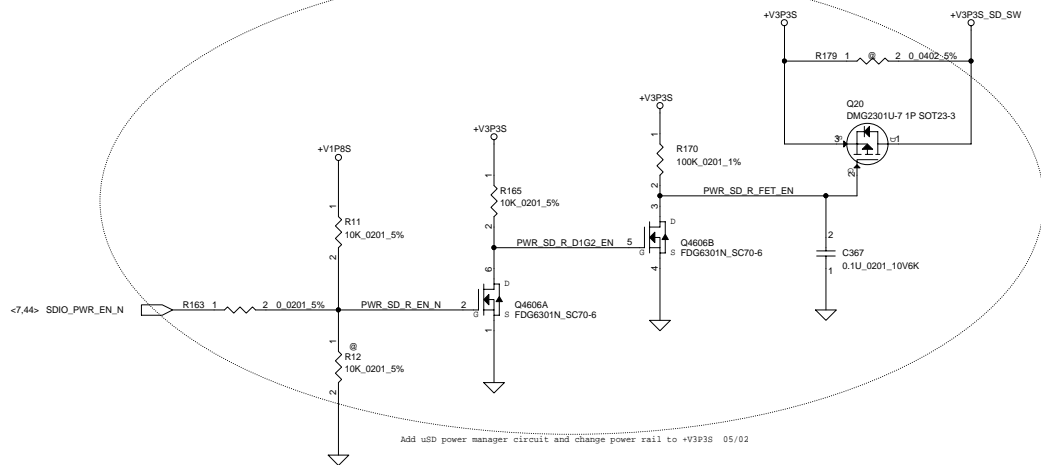
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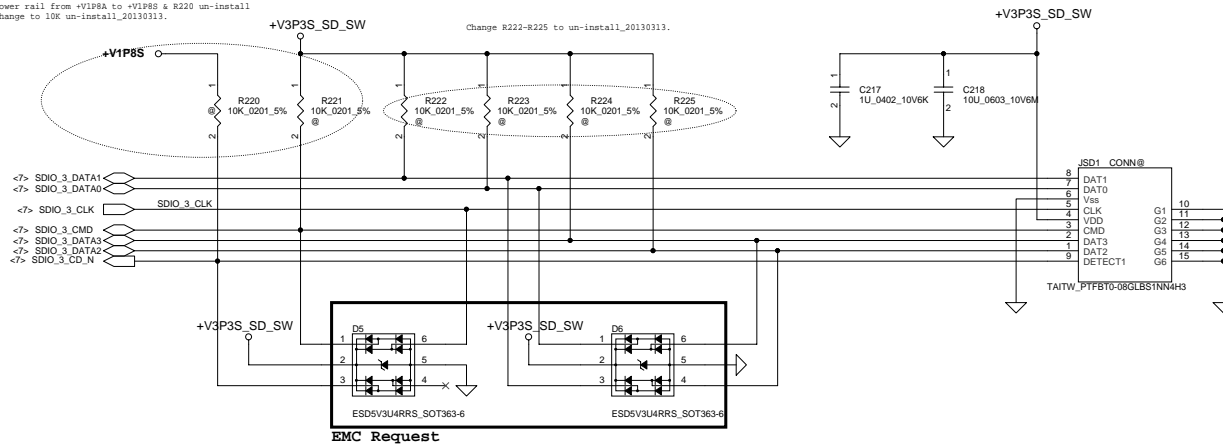
To1  
To2  
To3  
To4  
To5

#4- Mic  
#3, #5 - GND; 可選#3或#5其中1 Pin當GND, 另1 Pin則當Detect Pin  
#2- R  
#1- L  
MS- 無功能

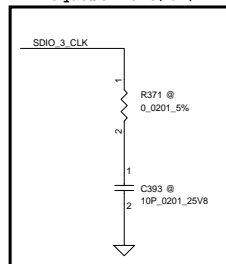
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/12/01	Deciphered Date	2015/12/01	Title	SCHEMATIC MB AA271	
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				Date:	Wednesday, August 21, 2013	Sheet 23 of 52



Change power rail from +V1P8A to +V1P8S & R220 un-install  
& R221 change to 10K un-install\_20130313.



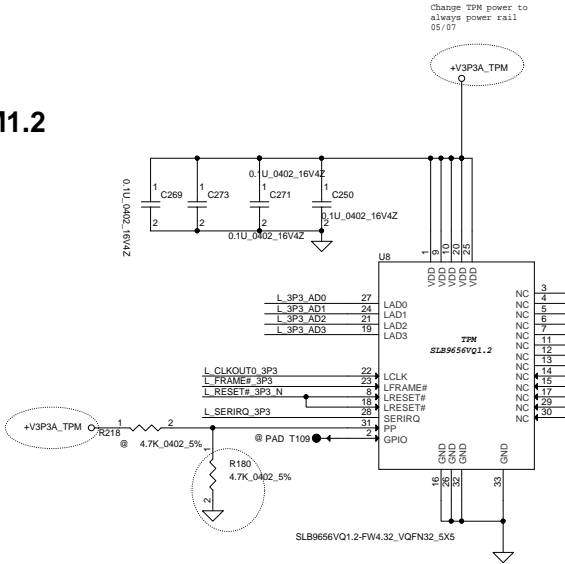
RF Request 2013/01/17



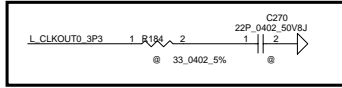
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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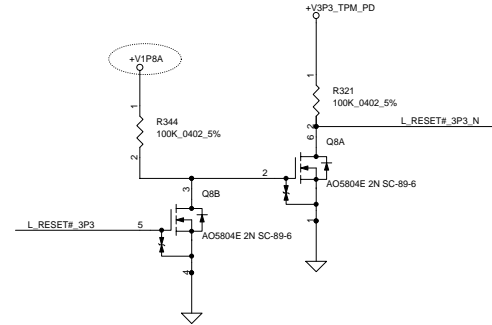
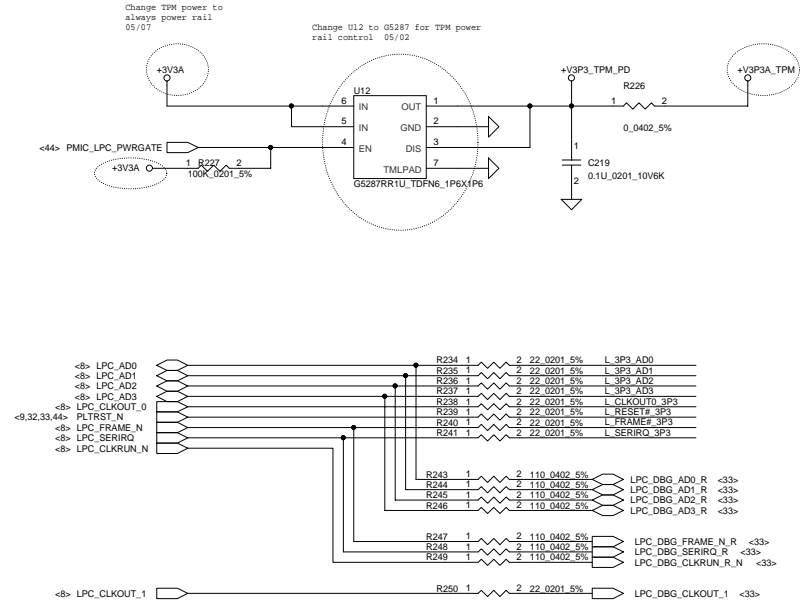
## TPM1.2



```
* Base I/O Address
  0 = 02Eh
  1 = 04Eh
```

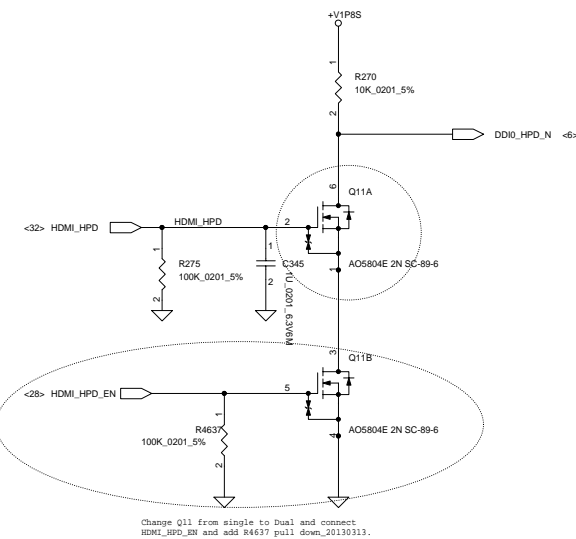
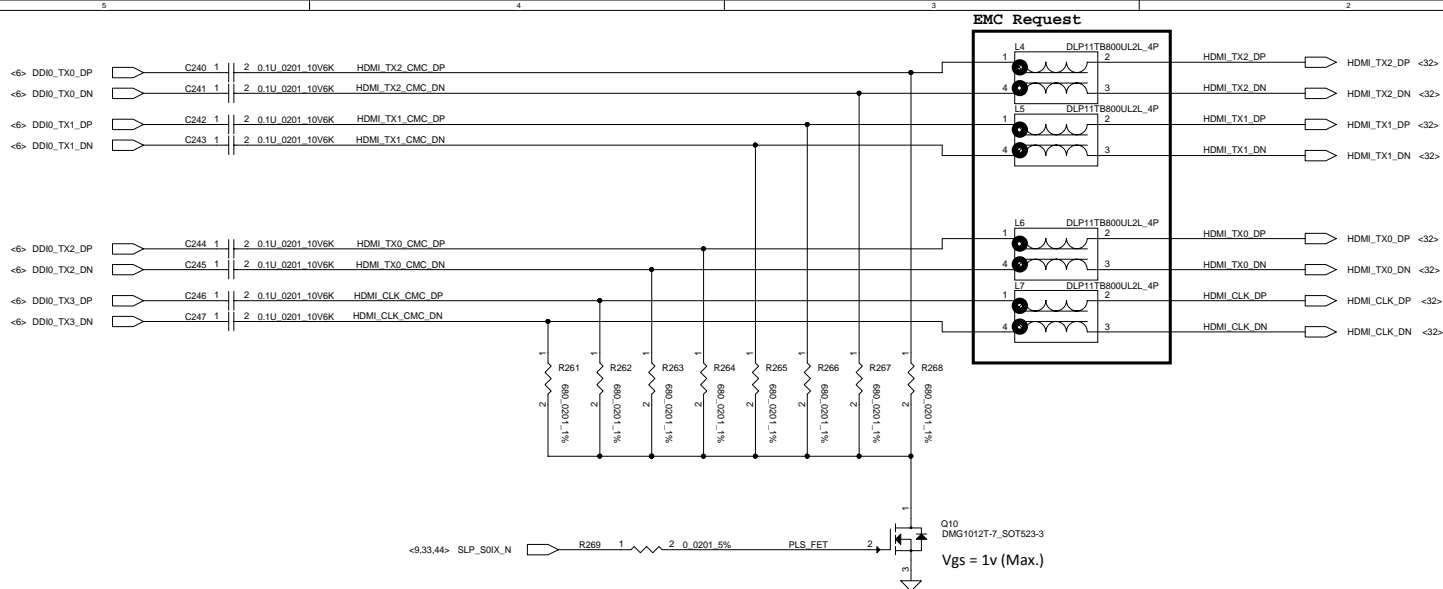


## EMC request

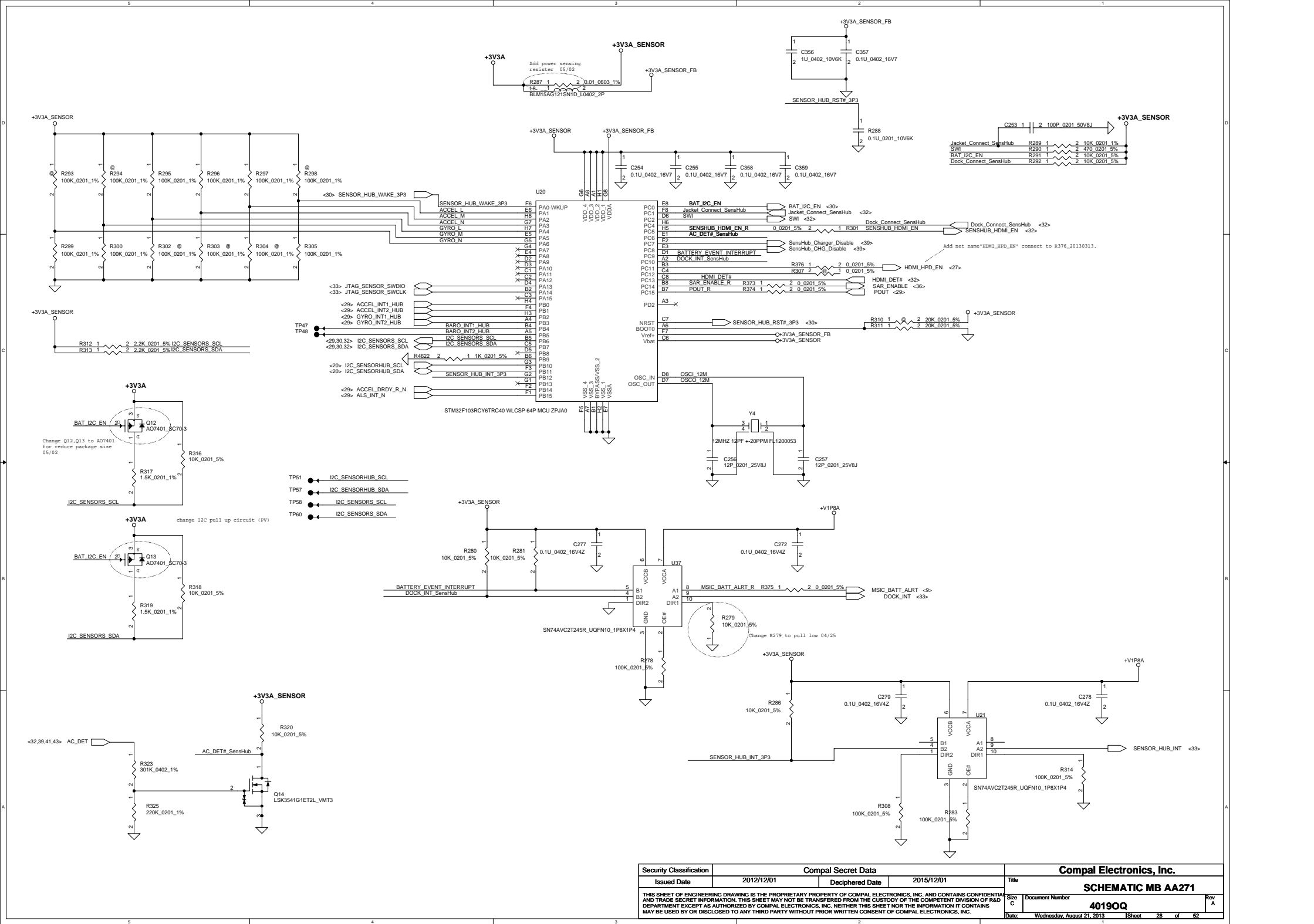


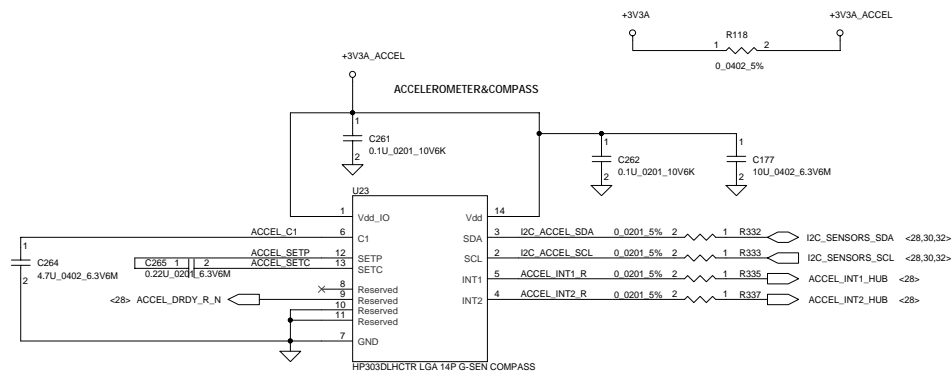
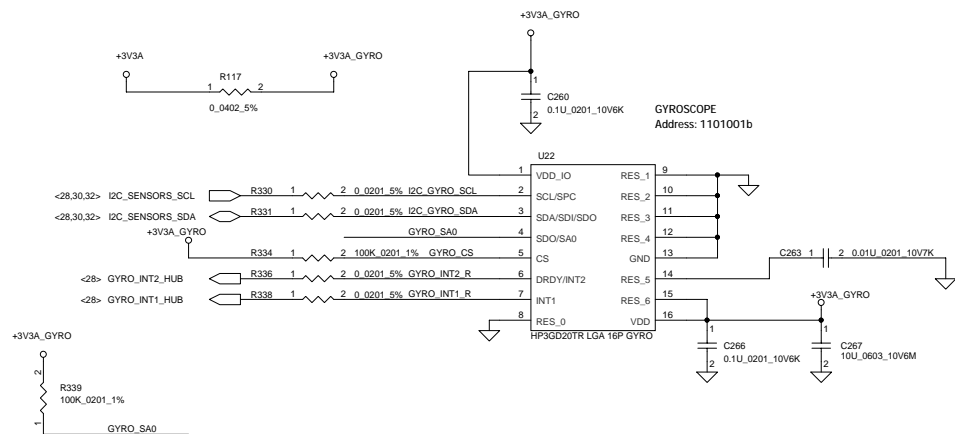
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				SCHEMATIC MB AA271				
				Size	Document Number			Rev
				40190Q			A	
				Date:	Wednesday, August 21, 2013		Sheet	25



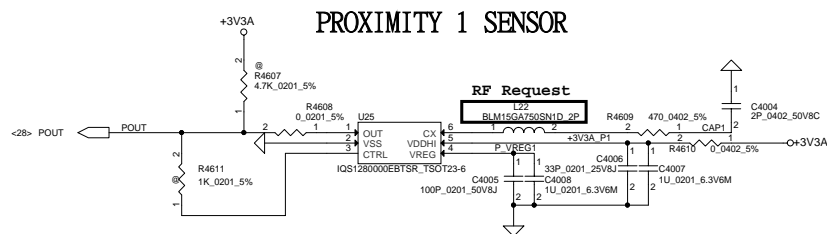
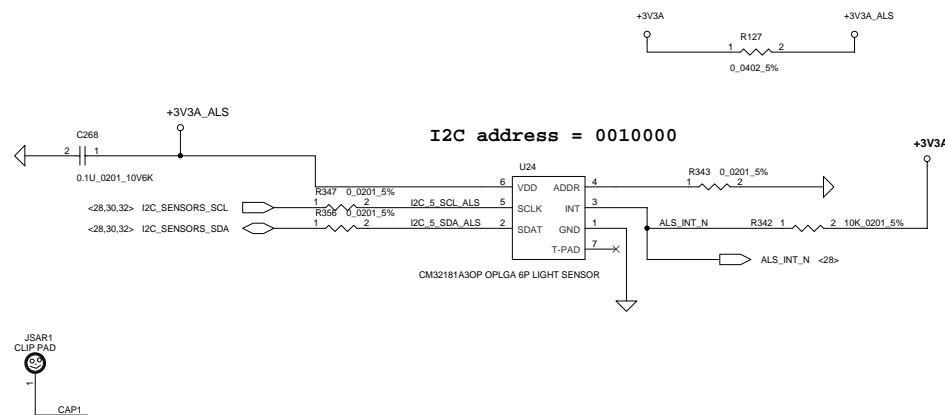


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								Size C	Document Number			40190Q		Rev A	
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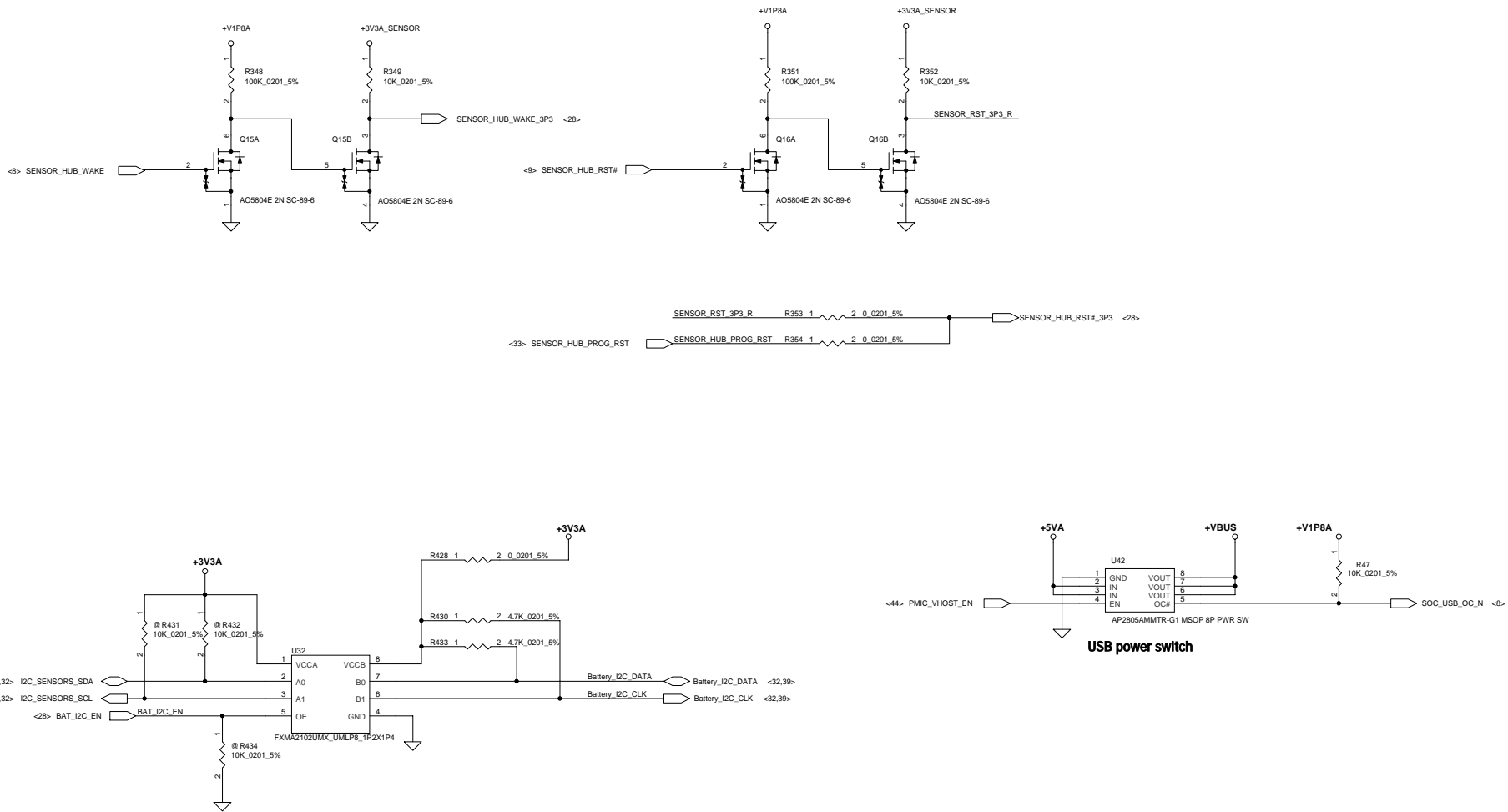




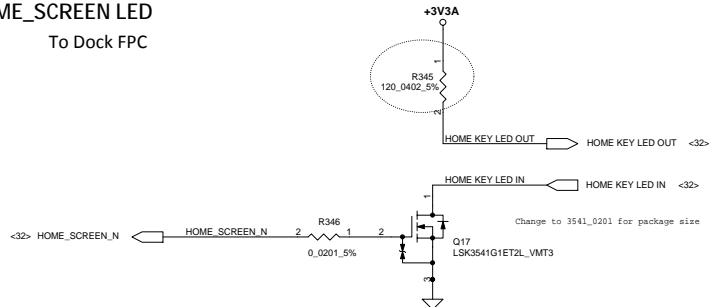
## LIGHT SENSOR



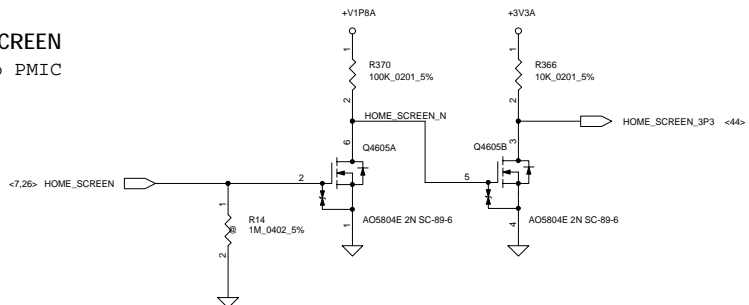
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## HOME\_SCREEN LED To Dock FPC

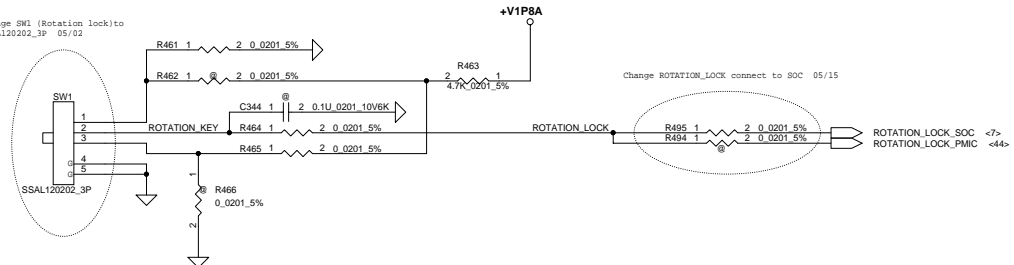


## HOME\_SCREEN To PMIC

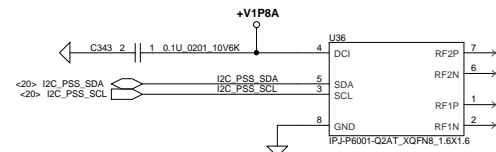


## ROTATION LOCK

Change SW1 (Rotation lock) to  
SSAL120202\_3P 05/02

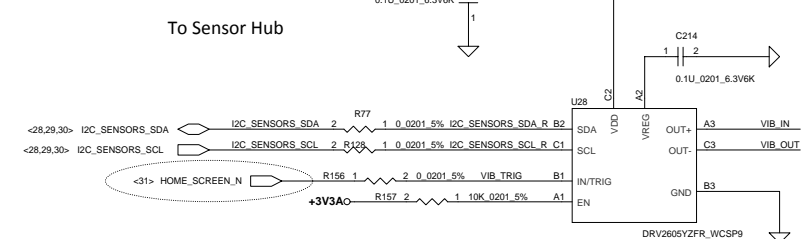
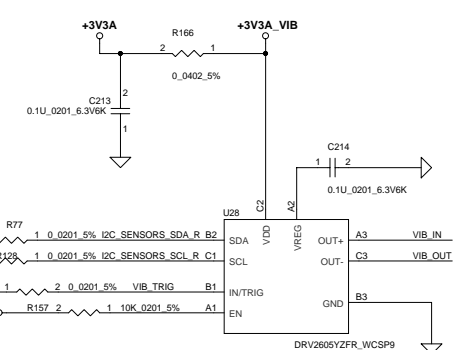
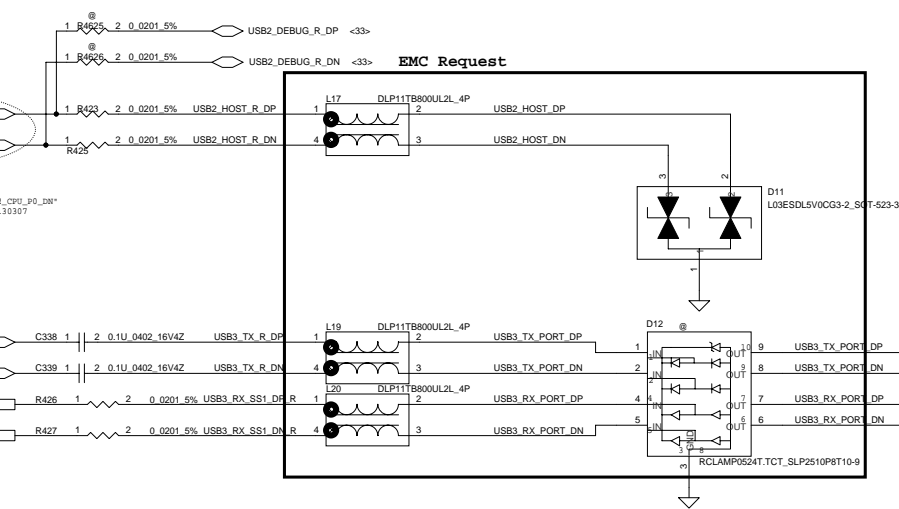
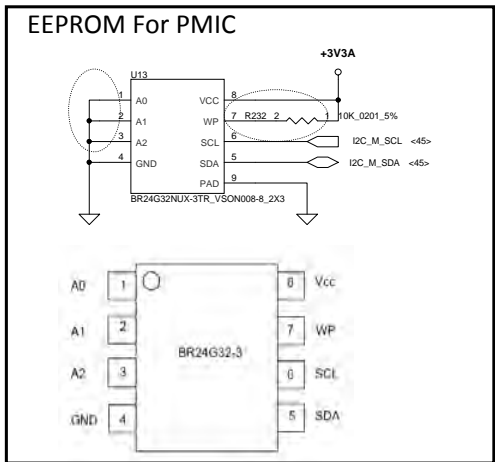
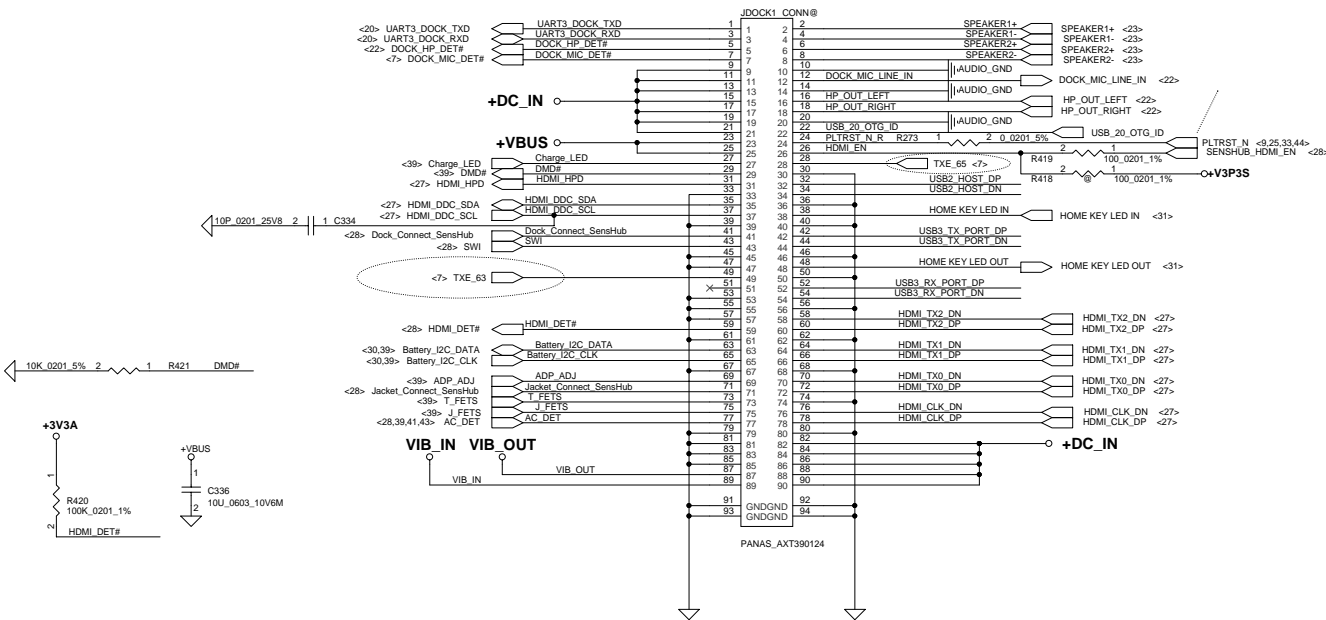


## PSS



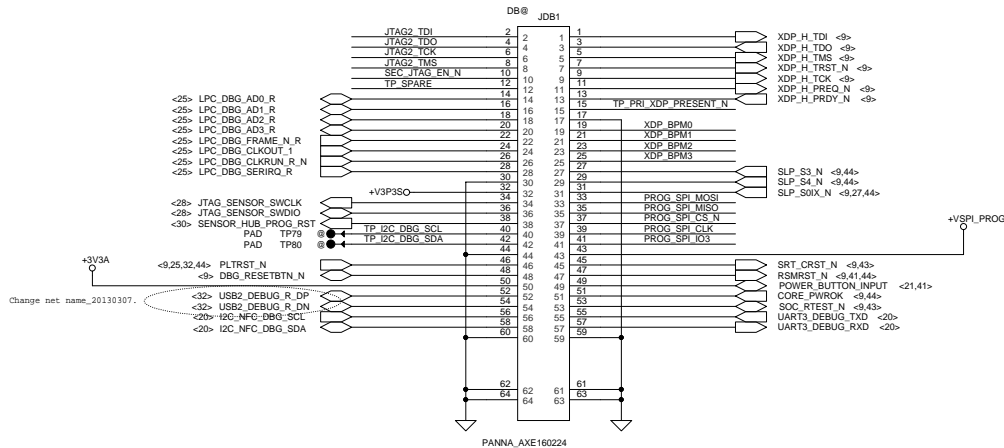
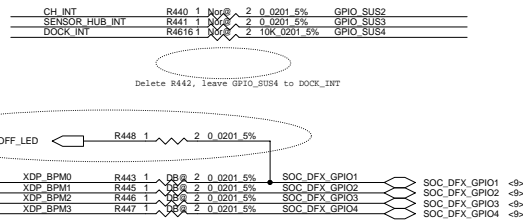
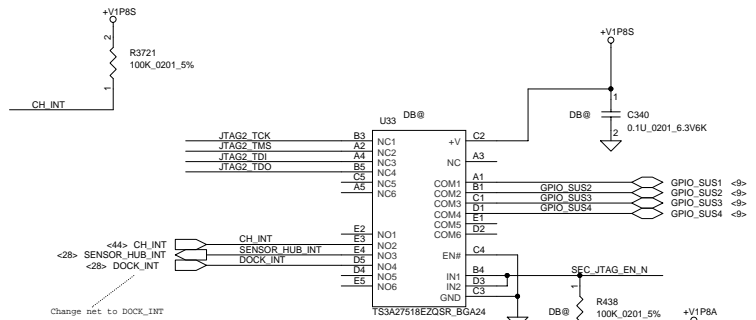
Remove PSS antenna circuit 2013/03/18

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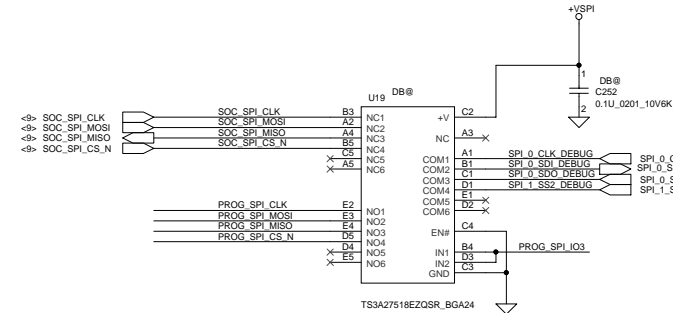
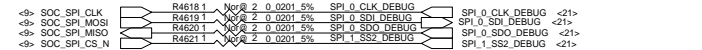
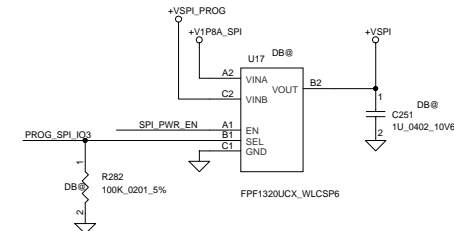
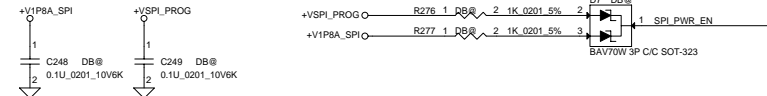




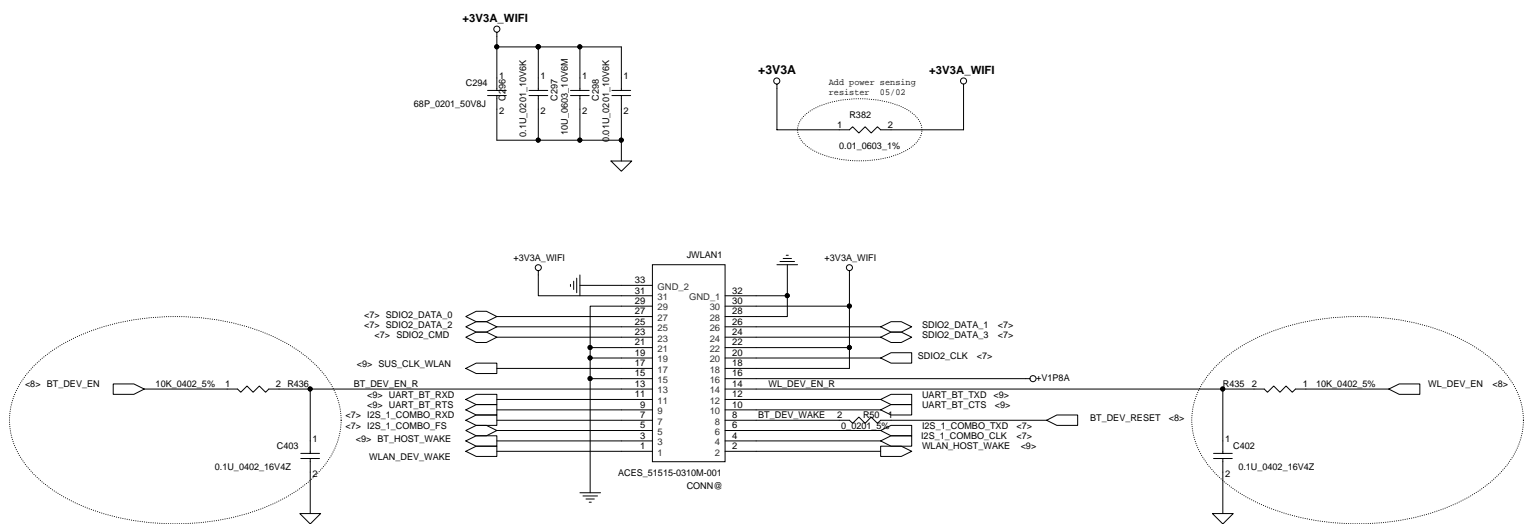
# INTEL DEBUG CIRCUITS FOR DEVELOPMENT PHASE



SPI POWER MUX DEFAULT--> LOW	
SEL = 0	+V1P8A from Platform
SEL = 1	+VSPI_PROG



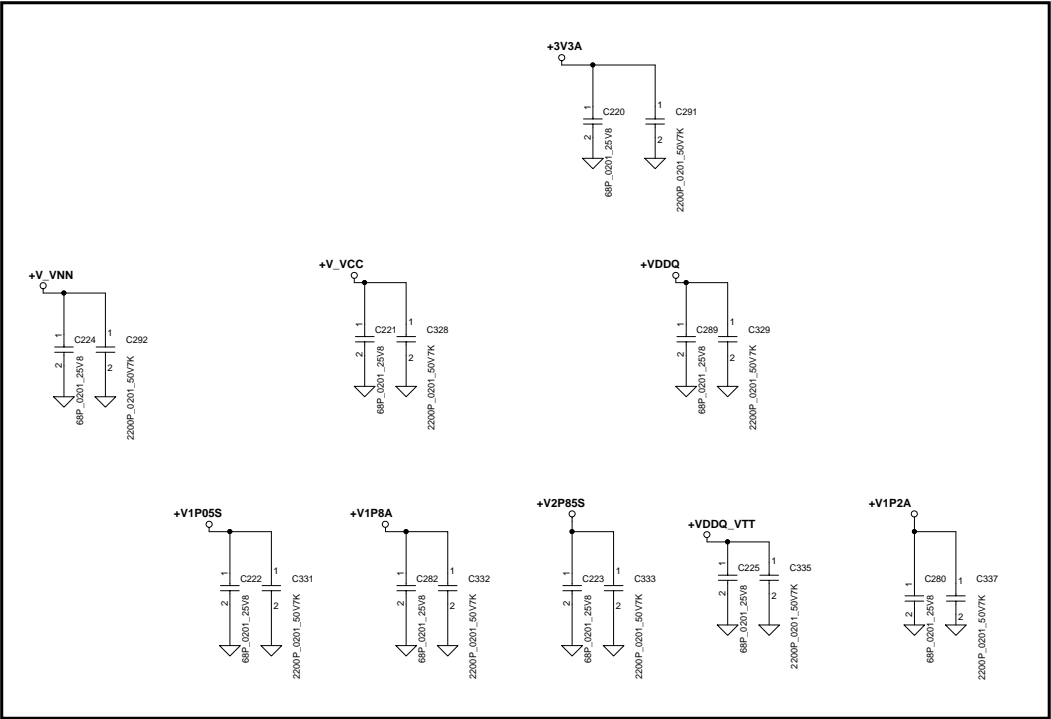
SPI MUX DEFAULT--> LOW	
IN1=IN2=0	SOC SPI Path
IN1=IN2=1	PROGRAMMING Path



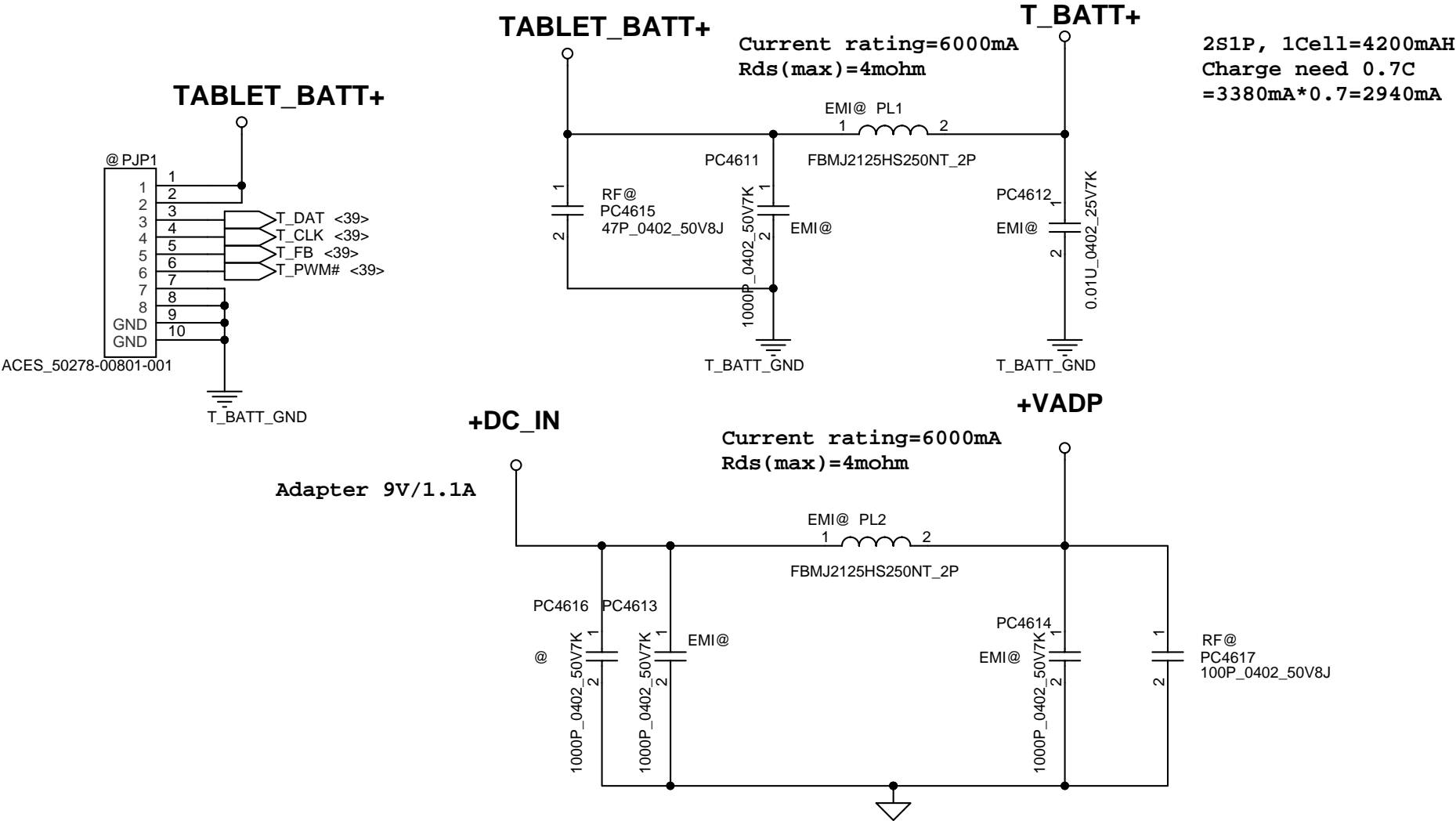




RF Request

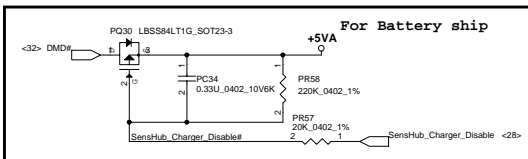
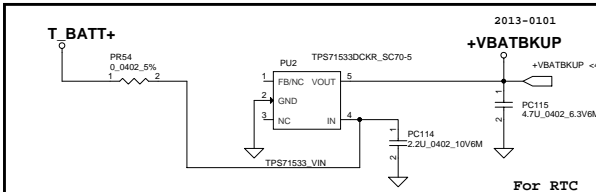
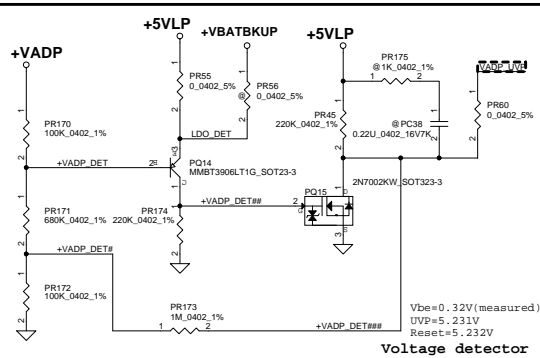
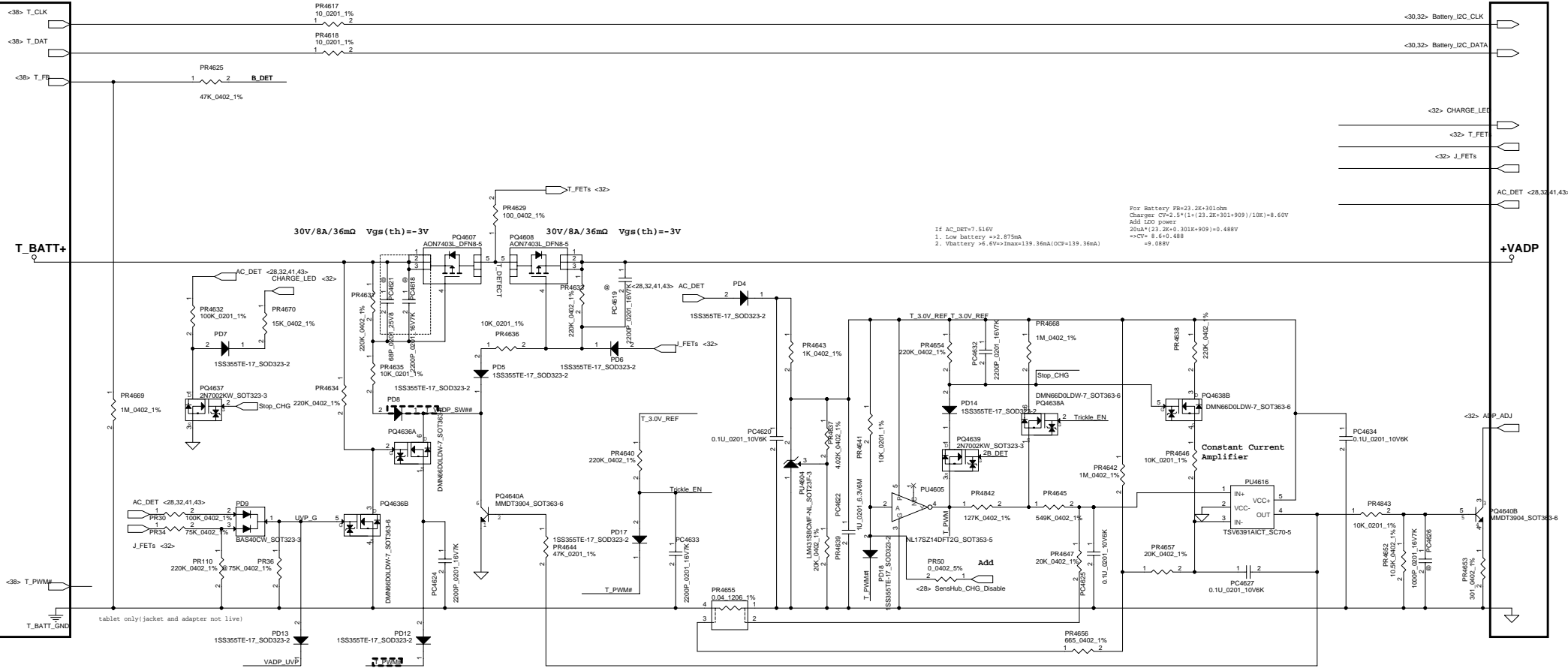


BATT/ADAPTER IN



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BATT Selector (TABLET)



只插DOCK	I<1.96A	I>1.96A
Low battery	7.516V	4.458V
Need charge	9.205V	5.411V
Charge finished or OCP/OVP	6.406V	3.801V

When AC\_DET is powered

	PWM	PWM#
Low power	0	OPEN(1)
Need charge	0-1	OPEN-0(1-0)
Charge finished	1	0

PQ17B與PQ9不會同時ON

	PQ17B	PQ9
Low power	ON	OFF
Need Charge	OFF	ON
Charge finished or OVP/OCP	OFF	OFF

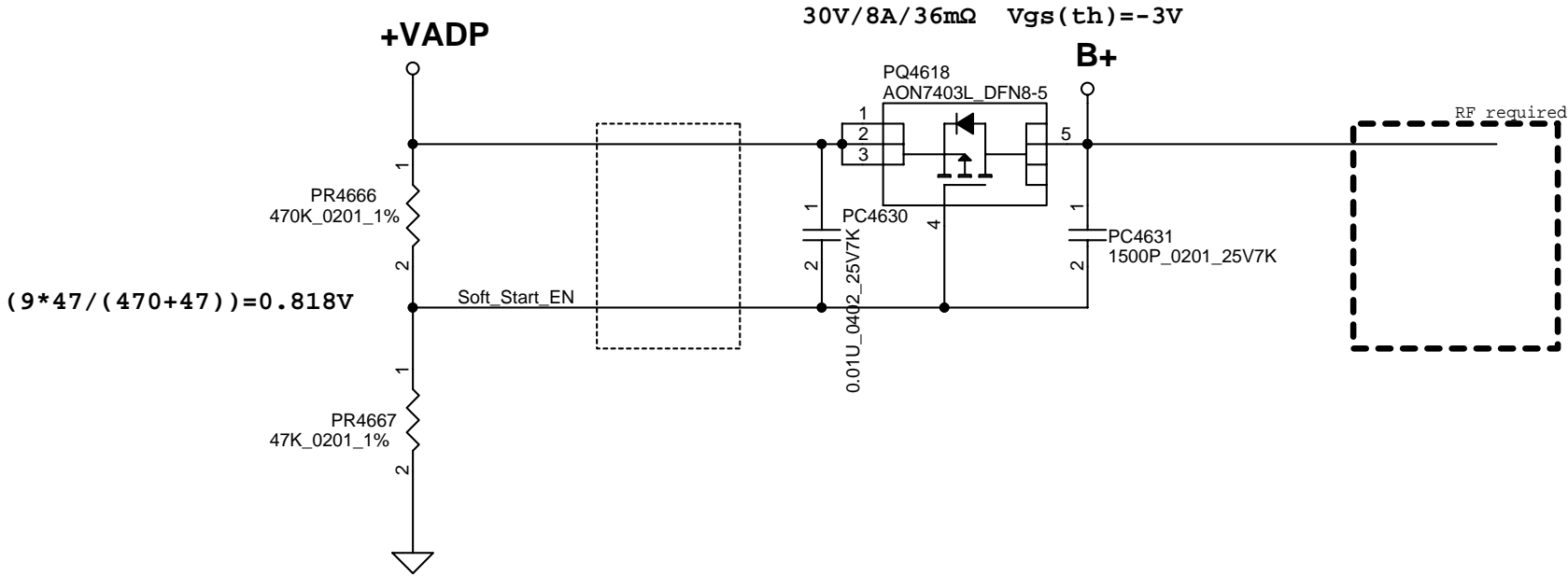
OCP or OVP will close PQ9

同時插Jacket與DOCK		+VADP	
Tablet	Jacket	I<1.96A	I>1.96A
Low battery	Low battery	8.058V	4.780V
Low battery	Need charge	9.234V	5.478V
Need charge	Low battery	9.234V	5.478V
Need charge	Need charge	9.234V	3.823V
Charge finished or OCP/OVP	Low battery	7.516V	4.458V
Low battery	Charge finished or OCP/OVP	7.516V	4.458V
Need charge	Charge finished or OCP/OVP	9.205V	5.411V
Charge finished or OCP/OVP	Need charge	9.205V	5.411V
Charge finished or OCP/OVP	Charge finished or OCP/OVP	6.406V	3.801V

Adaptor CP=1.96A BATTERY OCP 2.5V\*20K/(464K+20K) BATTERY OVP 2.5\*(battFB+100+10K)/10K=8.5V  
ADJ I<1.96A=>ADJ=6.33V =0.1033V If OVP=8.5V  
I>1.96A=>ADJ=3.758V 0.1033V/0.04=2.58A battFB=23.9K ohm

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				ISheet	39 of 62

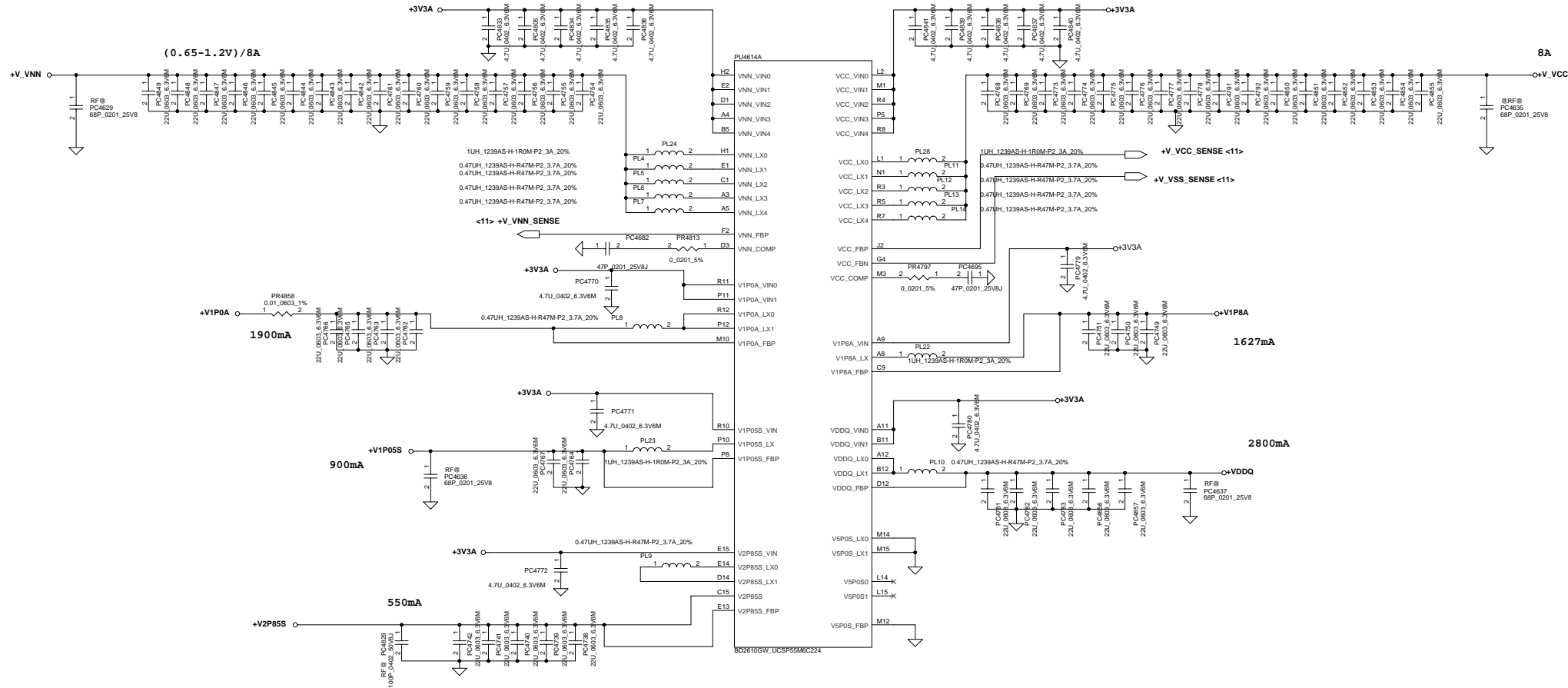
SOFT START



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				Size Custom	Document Number 40190Q	Rev A
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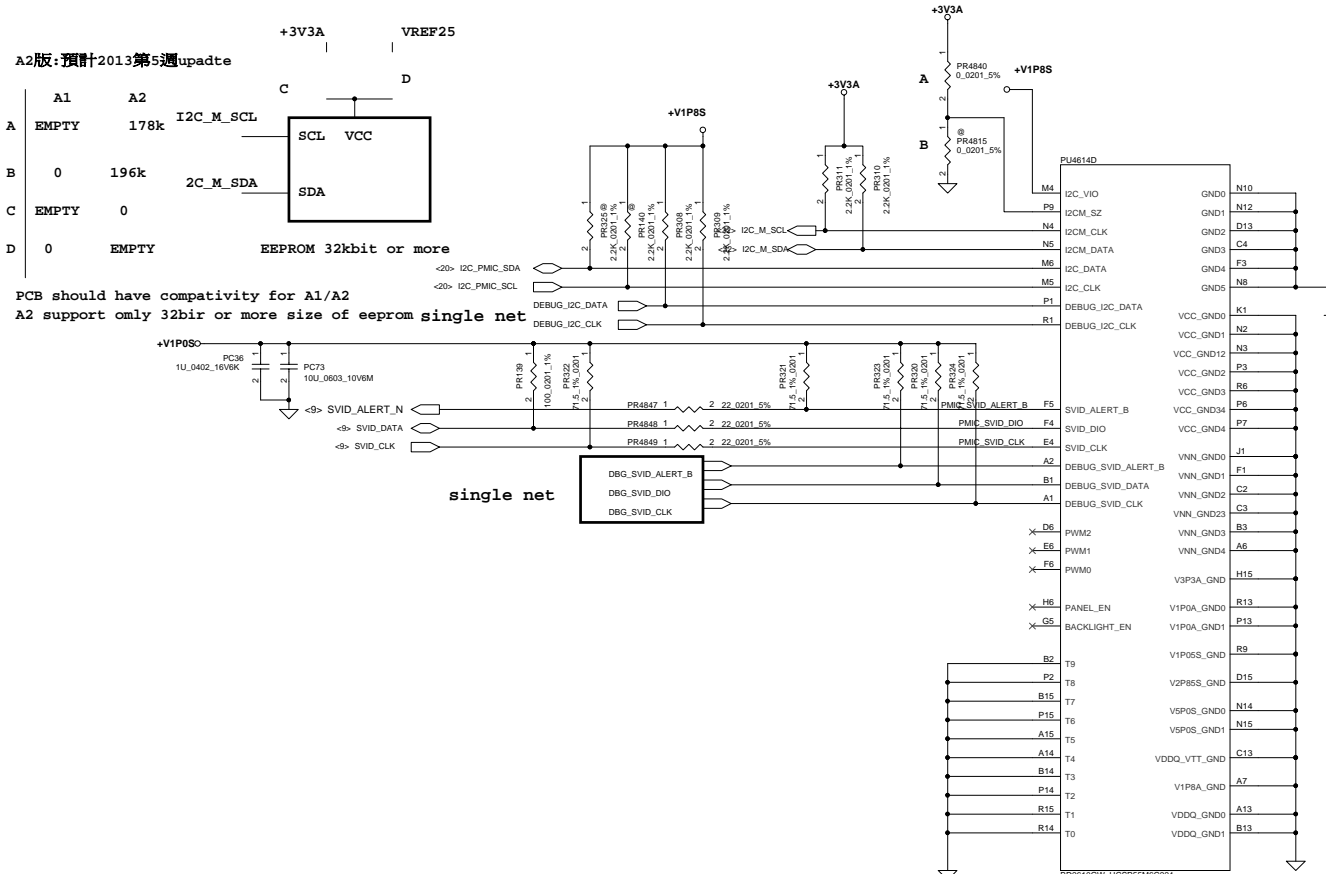












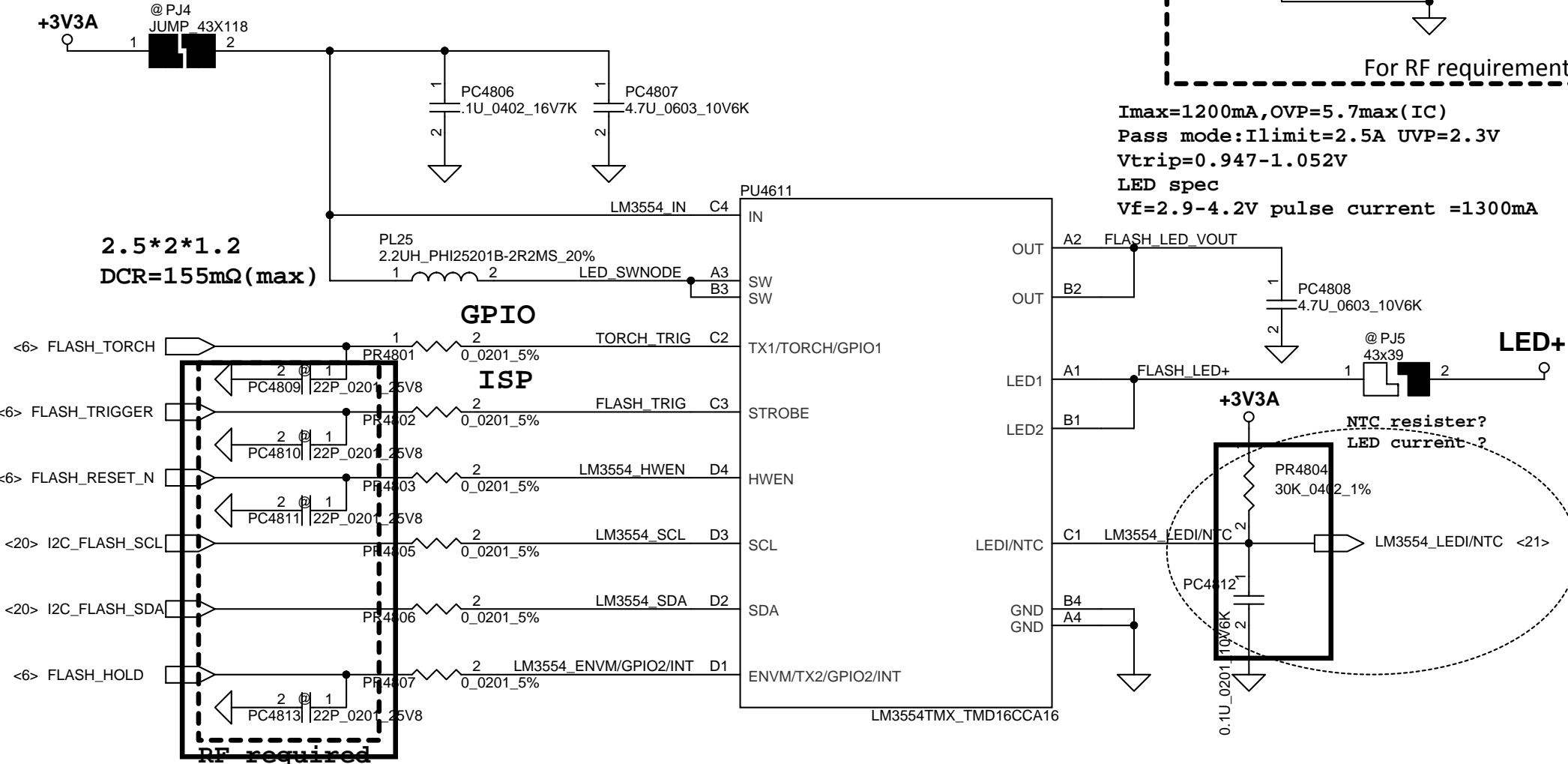
A2版:預計2013第5週update

	A1	A2
A	EMPTY	178k
B	0	196k
C	EMPTY	0
D	0	EMPTY

I2C\_M\_SCL  
I2C\_M\_SDA  
EEPROM 32kbit or more

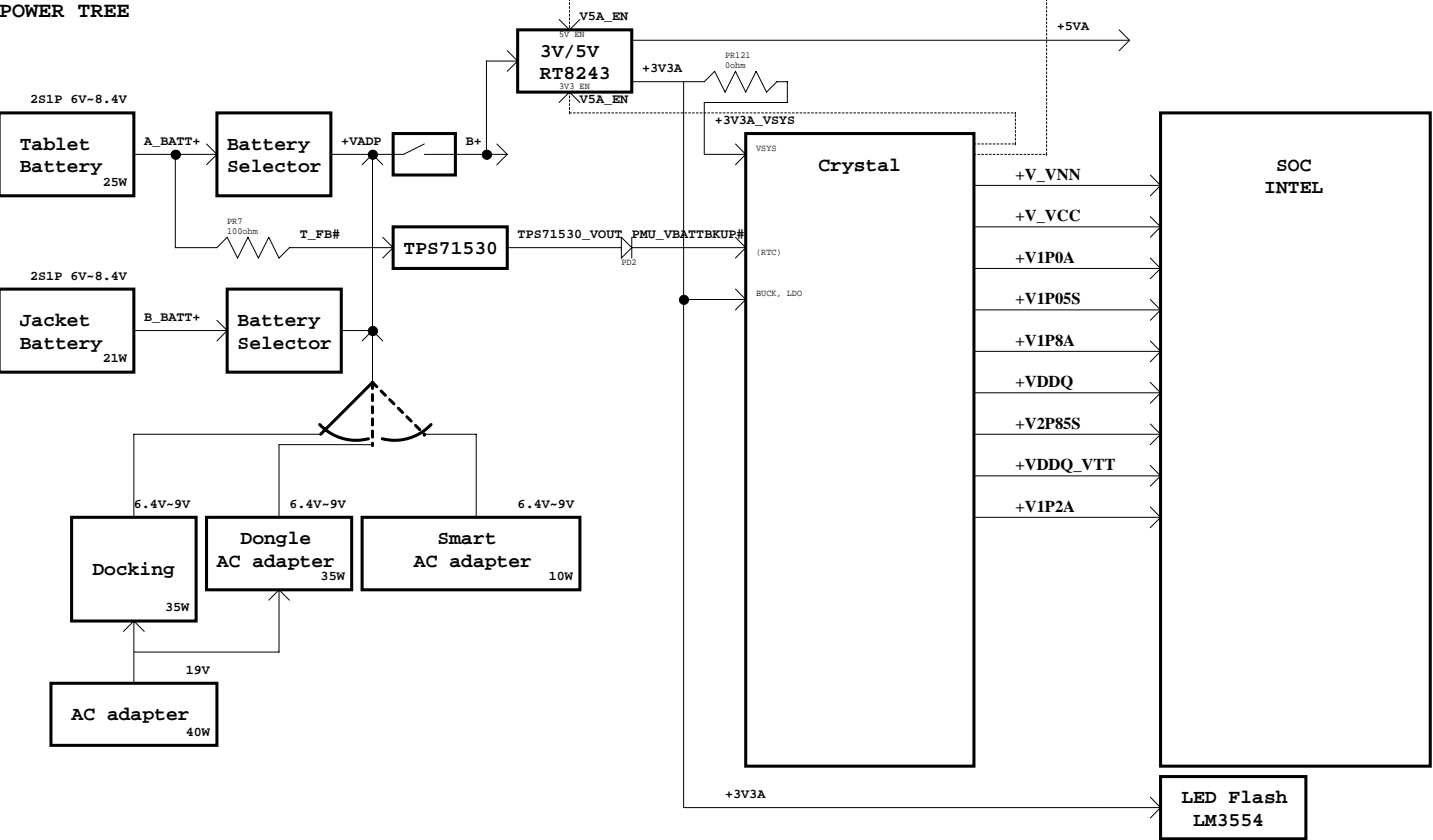
PCB should have compativty for A1/A2  
A2 support omly 32bir or more size of eeprom single net

LED Flash



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POWER TREE



Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	symbol link				1.PL4,PL5, PL6, PL7, PL9, PL10, PL11, PL12, PL13, PL14 =>LINK symbol	2012/12/24	
2	1.netname : for RTC 2.follow reference circuit 3.mos issue 4.remove EMI component 5.change netname 6.location changed 7.Cap changed 8.netname removed 9.netname changed 10.+V1P8A removed (重複) 11.netname changed 12.@ removed			P39 P41 P41 P41 P42 P43 P43 P43 P44 P45 P46	2.PMIC =>link 1.PMU_VBATBKUP# => +VBATBKUP 2.Reference circuit:module design (PR4818,PR4819,PR4821,PR4822,PR4832) 3.add PR4832 and PR4838 4.remove PC4828,PC4829,PC4831 and PC4832 5.VDDQ => +VDDQ 6.PQ4631B => PQ32B 7.PC4785(47u) => PC4785(22u) and PC4828(22u) 8.netname: (+V1P05X_PMIC) and (+V1P05_PMIC) removed 9.PMIC K12 pin (+V1P05X_SENSE) => +V1P05X PMIC L12 pin (+V1P05_PMIC) => +V1P05 PMIC J12 pin VDDQ => +VDDQ 10.add +3V3A circuit(PR4217,PR4218,PR4219,PR4220) 11..PMIC N5 pin 2C_M_SDA => I2C_M_SDA 12.PR4804 and PC4812	2013/01/01	
3	1.update battery selector(follow customer) 2.(22U_0603_6.3V6M)*2 =>10U_0402_6.3V (follow intel) P43 3.(follow intel) 4.(follow intel) 5.(follow intel) 6.(follow intel) 7.(follow intel) 8.(follow intel) 9.name changed Soc VSDIO_V3P3A_VIN(G3) 10.(follow intel) 11.(follow intel) 12.(follow intel) 13.(follow intel) P42 14.(follow intel) 15.(follow intel) 16.(follow intel) 17.(follow intel) 18.(follow intel) 19.(follow intel) 20.(follow intel) 21.(follow intel) 22.(follow intel) 23.(follow intel) 24.(follow intel) 25.(follow intel) 26.(follow intel)			P39 P43	1.add PR30,PR34,PD9,PR110,PR36,PR50 2.Delete PC4828,PC4785(10U_0805_16V6K) add PC4828 10U_0603_6.3V6M 3.Delete PC67,PC68 ,10U_0805_16V6K => 10U_0603_10V6M(PC64,PC65) 4.add PC35 1U_0402_10V6K 5.add PC4664 0.1U_0603_16V7 6.add PC4665 0.01U_0201_16V7 7.add PC4667 330P_0402_50V7K PR4756 10K_0201_1% 8.add PC310 0.1U_0603_16V7K 9.+3V3A => +V3P3A 10.add PC29 1U_0402_16 => 0.1U_0603_16V7K 11.Delete PC312(4.7U_0603_10V6K) PC309(0.1U_0603_16V7K) add PC312 10U_0603_6.3V6M 12.Delete PC33(1U_0402_16V6K) 13.47P_0603_50V8J => 47P_0402_50V8J (PC4682,PC4695) 14.1U_0402_16V6K => 0.1U_0603_16V7K (PC32) 15.2.2U_0603_10V6K => 1U_0402_10V6K (PC72) 16.10U_0603_25V6M => 1U_0603_10V6K (PC71) 17.1U_0402_16V6K => 0.1U_0603_16V7K (PC31) 18.1U_0402_16V6K => 0.1U_0603_16V7K (PC27) 19.1U_0402_16V6K => 00.1U_0603_16V7K (PC26) add 4.7U_0402_6.3V6M @ (PC74) 20.add PC36 1U_0402_16V6K 21.10U_0603_25V6M => 1U_0402_10V6K (PC70) 22.10U_0603_25V6M => 1U_0402_10V6K (PC69) 23.10U_0603_25V6M => 1U_0402_10V6K (PC68) 24.Delete low switch(VSYS_SX_EN_N),(VSYS_U_EN_N) 25.Delete 0.1U_0201_6.3V6K (PC4657) 26.Delete 0.1U_0603_16V7K (PC310)	2013/01/04	
4	1.(follow intel) 2.(follow intel) 3.(follow intel) 4.(follow intel) 5.(follow intel) 6.(follow intel) 7.(follow intel) 8.(follow intel) 9.(follow intel) 10.(follow intel) 11.(follow intel) 12.(follow intel) 13.name changed			P44	1.add PC311 0.1U_0603_16V7K 2.Delete PR303,PR304,PR305 3.add 10K_0201_1% @ (PR4731) 4.add 10K_0201_1% @ (PR4732) 5.Delete PC23 6.1U_0402_16V6K => 0.1U_0603_16V7K(PC24) 7.add 0.0402_5% (PR4844) 8.add 2.2U_0402_10V6M (PC73) 9.PC22 => @ 10.add 0.0402_5% @ (PR4845) 11.Delete V3P3U_EN_N 12.Delete 0.0402_5% (PR4800) 13.GPIOLP0_UIBTN_B(E7) HOME_SCREEN_FPC => HOME_SCREEN_3P3	2013/01/04	
5	1.(follow intel) 2.(follow intel) 3.(follow intel) 4.(follow intel) 5.(follow intel) 6.(follow intel) 7.(follow intel) 8.(follow intel) 9.(follow intel) 10.(follow intel) 11.(follow intel) 12.(follow intel) 13.name changed			P45	1.Delete 0.1U_0603_16V7K (PC308) 0.0402_5% (PR4812) 2.remove 0.0402_5% @ (PR4840) 3.I2C_CLK(M5),I2C_DATA(M5) need to check 4.DEBUG_I2C_DATA(P1),DEBUG_I2C_CLK(R1) need to check 5.SVID_ALERT_B(F5), need to check (PR321),add 22R_0201 6.SVID_DIO(F4),add (22R_0201)*2,(1k_0201) 7.SVID_CLK(R4),add (22R_0201)*1,need to check (PR322) 8.need to check DBG_SVID_ALERT_B(A2) 9.need to check DBG_SVID_DIO(B1) 10.need to check DBG_SVID_CLK(A1)	2013/01/06	
6	1.name changed 2.Delete low switch(follow intel) 3.follow Astro 4.name changed 1.followe customer 2.followe customer 3.followe customer 4.followe customer 5.followe customer 6.followe customer 7.followe customer 8.followe customer 9.followe customer 10.followe customer			P41 P44 P43	1.(LX_3V => TP851285_3V3_LX),(LX_5V => TP851285_5V_LX) 2.Delete V3P3U_EN_Ncircuit 3.1M_0402_1% => 100K_0201_1% ,(PR4790,PR4792) 4.+V3P3A => +3V3A 1.Add PC4666 (0.1U_0402_16V7K) 2.change PC4785(10U_0603_6.3V6M)(delete) => PC4858,PC4859(22U_0603_6.3V6M)(add) 3.change PC28 (0.1U_0402_16V7K) => PC28(1U_0402_16V6K) 4.add PC4672 (0.1U_0402_16V7K) 5.change PC68,PC69,PC70 (1U_0402_10V6K) => PC68,PC69,PC70 (10U_0603_10V6M) 6.change PC27,PC31(0.1U_0402_16V7K) => PC27,PC31(10U_0603_10V6M) 7.change PC71(1U_0402_10V6K) => PC71(10U_0603_10V6M) 8.add PC32(1U_0402_16V6K) 9.add PC33(1U_0402_16V6K) 10.change PC29(0.1U_0402_16V7K) => PC29()		

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	1.NET NAME CHANGE 2.delet PQ4641 NTS4001NT1G 1N_SC70-3 3.delet PR4854 0_0402 5% 4.add PR310,PR311 2.2K_0201_1% 5.bom change 0201==>0402 PR4647,PR4657 6.PR4787 100K_0201_5%==>100K_0201_1% unpop 7.PR4788 100K_0201_5%==>100K_0201_1% unpop 8.add PR310,PR311 2.2K_0201_1%	DB0=>DB1			2.Rohn suggest 3.Rohn suggest 4.Rohn suggest 6.Rohn suggest 8.Rohn suggest	2013/1/15	
2	1.Remove PL21, PC4784, PD53, PC4743-PC4748	DB0=>DB1	42		1.Remove PU4614 +V5P0S this power rail by Customer request	2013/3/13	
3	1.Change PC4615 from 1000pF to 47pF 2. Add PC4623 and non-POP (0201 pad) 3. Add PC4628 and non-POP (0201 pad) 4. Add PC4629 and non-POP (0201 pad) 5. Add PC4635 and non-POP (0201 pad)	DB0=>DB1	38 41 41 42 42		1-5.By customer's request	2013/3/13	
4	1.Delete PR4853 2.Pop PR4852	DB0=>DB1	43		1.Remove PU4614 +V5P0S this power rail and change +VHDMI input source by Customer request	2013/3/14	
5	1. Change PR4789 from 100k Ohm to 47k Ohm 2. Depop PC4665 & PC4667 3. link PL1 & PL2 symbol	DB0=>DB1	43		1-2. By customer's request	2013/3/14	
6	Change PQ4637 & PQ4639 from SB000005N00 ( NTS4001NT1G 1N SC70-3) to SB000009Q80 ( S TR 2N7002KW 1N SOT323-3) (HP request)	DB0=>DB1	39		1. By customer's (Tom)request	2013/3/27	
7	1.Change PJ6 from (PR4853) 0.01_0603_1% 2.Add PR4857(0.01/0805) on +3V3A output 3.Add PR4858 (0.01/0603) on +V1P0A	DB1=>SI1	41 41 42		1. intel's request 2. intel's request 3. intel's request		
8	1.Change netname B+ from +3VLP on PR4831 2.Add 220K_0402_1% on PR4856 and PR4854 3.Change netname TPS51285_VIN# from TPS51285_EN on PC4830 4.Change netname TPS51285_VIN# from B+ on PC133 5.Change netname TPS51285_VIN# from TPS51285_EN on PR4824 6.Change netname TPS51285_VIN# from TPS51285_EN on PR4841	DB1=>SI1	41 41		1. customer's request 2. customer's request 3. customer's request 4. customer's request 5. customer's request 6. customer's request		
9	1. Add a 0201 pad on V1P05S, near PMIC (PC4636) 2. Add a 0201 pad on VDDQ, near PMIC (PC4637) 3. Add a 0201 pad on V_VNN, near PMIC (PC4629 can be used) 4. Add a 0201 pad on V1P8S, near PMIC (no enough area) 5. Add a 0201 pad on V1P2A, near PMIC (PC4638)	DB1=>SI1	42		1. customer's request	2013/5/13	
10	1. Add PD19 and remove PR4825	SI1=>SI2	41		1. For PU4612 hot-plug leakage issue		
11	1. Change PU4614 G10(VSYS_SX_FB), G11(VSYS_U_FB), G12(V3P3U_FB), L6(ULPT_VBUS_EN) pin to GND	SI1=>SI2	43		1. For Rohm's suggestion		
12	1. Change PR4847, PR4848, PR4849 to 22ohm (SD00000LF80) 2. Change PR321, and PR323 change to 71.5 ohm Change PR139 to 100 ohm	SI1=>SI2	45		1&2. For Rohm's suggestion		
13	1. Change PC4816, PC4617 to 100pF & RF@ 2. Add PC4829, PC4831 100pF & RF@ 3. Change PC171, PC172 from 22pF to 68pF	SI1=>SI2	38		1-3. For RF's request		
14	1. Add PC4639, PC4640 0201 pad & @RF@	SI1=>SI2	41		1.For RF's request		
15	1. Remove PD19 & PR164 2. Change PMIC_PG met name to TPS51285_PD_IC 3. Change PR4809 to 10 kohm 4. Change PR160 to 200kohm	SI1=>SI2	41		1.Reduce PU4612 delay circuit		
16	1. Change PR4842 to 127k 2. Change PR4645 to 549k	SI1=>SI2	39				

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1	2013/03/07	6		Intel suggest	U3.BC9 & U3.BB10 connect to GND directly.	DB1	
2	2013/03/07	7		Intel suggest	Reserve R4627(4.7K) for U3.BK36(I2S_2_TXD) pull down.	DB1	
3	2013/03/07	8		Customer request	Del "USB2_CPU_P0_DP" & "USB2_CPU_P0_DN" let NC	DB1	
4	2013/03/07	21		Intel suggest	Let U7.4 NC	DB1	
5	2013/03/07	21		For BIOS +1.8V use	Change JPWR1.4 from +3V3A to +V1P8A	DB1	
6	2013/03/07	26		Intel suggest	Exchange R252 & R254	DB1	
7	2013/03/07	32		Customer request	Change net from "USB2_CPU_P0_DP" & "USB2_CPU_P0_DN" to "USB2_DEBUG_DP" & "USB2_DEBUG_DN"	DB1	
8	2013/03/07	32		Customer request	Add R4625 & R4626 for Debug conn path	DB1	
9	2013/03/07	33		Customer request	Change JDB1.52 & JDB1.54 net name	DB1	
10	2013/03/12	32		Customer request	Add VIB_IN & VIB_OUT on JDOCK1.49 & 51 pin for 2nd vibrator_20130312.	DB1	
11	2013/03/12	35		Factory request	Change L16 & L18 footprint to follow vensor spec.	DB1	
12	2013/03/12	23		ME request	Change JLINE1 conn footprint & Pin 1 location	DB1	
13	2013/03/12	35		ME request	Change JNFC1 conn footprint & Pin define	DB1	
14	2013/03/12	21		ME request	Change JPWR1 conn footprint & Pin define	DB1	
15	2013/03/12	20		Customer request	Add R4630 & R4631;R4632 & R4633 pull high resistor for customer request.	DB1	
16	2013/03/12	8		Customer request	Reserve R4629 & R4628 pull high resistor for customer request.	DB1	
17	2013/03/12	26		ME request	Change JEDP1 conn footprint for ME request.	DB1	
18	2013/03/13	8		Customer request	Reserve R4635 & R4636 pull high resistor for customer request_20130313.	DB1	
19	2013/03/13	21		Intel suggest	Del R163 & R165	DB1	
20	2013/03/13	21			Add C4021(22nF) on U7.4 & update U7 symbol & footprint & reserve R4634 pull down resistor(100k) on U7.3	DB1	
21	2013/03/13	24			Change power rail from +V1P8A to +V1P8S & R220 un-install & R221 change to 10K un-install & Change R222~R225 to un-install.	DB1	
22	2013/03/13	27			Change Q11 from single to Dual and connect HDMI_HPD_EN and add R4637 pull down.	DB1	
23	2013/03/13	28			Add net name"HDMI_HPD_EN" connect to R376.	DB1	
24	2013/03/13	27			Change U16 to PCA9306 for HDMI DDC level shift (change R327/R328 to 47k, delete R329, R359, add R51, C147, C216)	DB1	
25	2013/03/18	31			Remove PSS antenna circuit (Delete L14, L15, C4019, C4020, JPSS1)	DB1	
26	2013/03/19	22		For Audio JD pin definition	1. Delete R558, R1779, R1780 2. Connect JACK_DET_N to U3E.T2(GPIO_S5_37), depop R207 3. Delete R442, leave GPIO_SUS4 to DOCK_INT 4. Change netname of I2S_INT# to DOCK_HP_DET#_R, connect to U3F.C21(GPIO_S5_14) 5. Connect DOCK_MIC_DET# to U3E(GPIO_S5_43) 6. Remove R4615; change U33.D5 to DOCK_INT	DB1	
27	2013/03/19	26		For Panel Power sequence fine-tune	Depop R4006, Pop R4007	DB1	
28	2013/03/19	26			Remove DDI1_TX2 & DDI1_TX3 and all the related component	DB1	
29	2013/03/19	28		For Sensor hub HDMI control	Pop R376 and Connect Jacket_Connect_SensHub directly to R289.1	DB1	
30	2013/03/19	35		For NFC filter circuit	Change C317 and C319 from 180pF to 270pF	DB1	
31	2013/03/19	21			Modify JPWR1 pin difinition for new connector	DB1	
32	2013/03/21	36			Swap UART_TX and RX for 3G module	DB1	
33	2013/03/21	21		For 8M camera reset pin control	Add R88 to connect CAM_PWDN with MCSI_GPIO_09	DB1	
34	2013/03/22	35		RF team request	Depop R406 and change R407 to 0 ohm	DB1	
35	2013/03/22	23		EMI team request	Reserve C226 on MIC_JACK	DB1	
36	2013/04/02	13		For pass Intel TIE simulation	Add C227, C228, C229, C281, and pop C352 Change C35, C45, C59 to 0.47uF and pop	DB1	

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Item	Date	Page	Fixed Issue	Reason for change	Modify List	Phase	Modify by
37	2013/05/02	12		Intel request	Add the multiplexer circuit for DDRIO power rail control	SI1	
38	2013/05/02	24			Add uSD power manager circuit and change power rail to +V3P3S	SI1	
39	2013/05/02	21			Change U6 to GMT G9184 for camera 1.2V power rail	SI1	
40	2013/05/02	25,26			Change U12, U14, U4002 to G5287 for power rail control	SI1	
41	2013/05/02	35			Change C316, C321 to 39pF, Change C318, C320 to 6.8pF, Change C323, C324 to 68pF, No install C394 and C395, Change C396 and C397 to 82pf	SI1	
42	2013/05/02	25			Change R180 to 4.7k	SI1	
43	2013/05/02	28			Change U37 pin10 to 10k pull low for BATTERY_EVENT_INTERRUPT signal direction reverse	SI1	
44	2013/05/02			for evaluation	Add power sensing resister R272,R217,R253,R219,R287,R382,R384	SI1	
45	2013/05/02	31		HP ME request	Change SW1 (Rotation lock)to SSAL120202_3P	SI1	
46	2013/05/02	28		For PCB space addition	Change Q12,Q13 to A07401 for reduce package size	SI1	
47	2013/05/02	26			Change homekey power rail to +VIP8S	SI1	
48	2013/05/02	21		Follow FFRD 1.5	Pop R490,R493 for Volume signal control	SI1	
49	2013/05/07	25			Change TPM power rail to +V3P3A	SI1	
50	2013/05/07	35			Pop NFC antenna boost circuit	SI1	
51	2013/05/07	13			Change C34, C43, C45, C57, C58, C229 decoupling cap to +V1P0SX_S power rail	SI1	
52	2013/05/09	36			Change NGFF pin difinition and add GPS_POWER_ON pin for Standalong GPS	SI1	
53	2013/05/10	26			Change homekey power rail to +V1P8A	SI1	
54	2013/05/10	21			Change Camera LED PN to SC50000A300	SI1	
55	2013/05/10	21			Add R4010 0 ohm for panel sequence fine tune	SI1	
56	2013/05/13	36			1. Re-route R322.2 (GPS_WAKEUP) to R417.2 (GPS_DISABLE#), rename to GPS_DISABLE# 2. Add 0ohm resistor connections on J3G1.34 AND J3G1.36, reserve for testing	SI1	
57	2013/05/13			For RF noise solution	1. Add a 0201 pad on V1P05S, near PMIC 2. Add a 0201 pad on VDDQ, near PMIC 3. Add a 0201 pad on V_VNN, near PMIC 4. Add a 0201 pad on VIP8S, near PMIC 5. Add a 0201 pad on VIP2A, near PMIC 6. Add a 0201 pad on PLT_CLK0_CAM1, near JPWR1 7. Add a 0201 pad on PLT_CLK1_CAM2, near JCAM1	SI1	
58	2013/05/14	07		For INTEL Audio driver BSOD issue	1. Re-connect R86.2 (JACK_DET_N) to U3D.BK14 (GPIO_S0_0) 2. Re-connect R4615.2 (DOCK_MIC_DET#) to U3D.BT10 (GPIO_S0_3)	SI1	
59	2013/06/03	35		Follow HP comm team recommend	Change NFC boost circuit to enlarge the BJT package size, along with 1210 resistor.	SI2	
60	2013/06/03	25			change TPM power source name to +3V3A	SI2	
61	2013/06/20	15			Add R187, R190 and memory config pin for memory size information	SI2	
62	2013/06/20	36			Add a 0ohm/Test Point @J3G1.32	SI2	
63	2013/06/20	31			1. Change net name "nHOMEKEY" to "HOME_SCREEN" 2. Divert R346.2 to R370.2, name "HOME_SCREEN_N"	SI2	
64	2013/06/20				1. Rename segment from U28.C2 to R166.1 to +3V3A_VIB 2. Rename +3VS_WIFI to +3V3A_WIFI 3. Rename +V3P3A to +3V3A 4. Rename +3V_HP to +V3P3S_HP 5. Rename +3VS_P1 to +3V3A_P1	SI2	
65	2013/06/25	26 44		Follow FFRD 1.5	1. Connect PU4614C.F9 (GPIO1P3) to U14.4 (replace SLP_S0IX_N) 2. Change R271 to 100K and pop	SI2	
66	2013/06/25	21		Follow FFRD 1.5	1. Connect +V1P8SX_CAM to U7.3 (EN) (replace SLP_S3_N) 2. Pop R4634	SI2	

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67	2013/07/01	21			Add R229 10K PD to GND on CAM_ACTIVITY_LED	SI2	
68	2013/07/01	21			Add R448 and connect GPIO_S5_23 to Q3 to control front LED when power off	SI2	
69	2013/07/01	7			<del>Connect I2S_2_TXD to 70pin Docking Conn Pin23 through a 0ohm resistor.</del> <del>..(connect I2S_2_TXD to JDOCK1_49 on M/B side).....</del>	SI2	
70	2013/07/03	35			Change R4623 from 24.9 +-1% 1210 to 6.1 +-1% 1210 Change value of C317 and C319 to 100pF Change value of C316 and C321 to 150pF Change value of C318 and C320 to 68pF pop all NFC boost component	SI2	
71	2013/07/03	36			Connect GPS_POWER_ON through a 0ohm resistor to J3G1.48, depop the 0ohm resistor (add R379)	SI2	
72	2013/07/03	32			Add Q21 for reverse HOME_SCREEN signal to trigger vibrator drive IC	SI2	
73	2013/07/04	7			1. Connect U3D.BT36 (I2S_2_FS) to 70pin Docking Conn Pin23 through a 0ohm resistor, pop 2. Connect U3D.BK36 (I2S_2_TXD) to 70pin Docking Conn Pin24 through a 0ohm resistor, pop 3. Connect U3F.H20 (PLTRST_N) to 70pin Docking Conn Pin26 through a 0ohm resistor, pop	SI2	
74	2013/07/04	44			Pull out PU4614C.E10 (PMIC_MEMCFG1) to +3V3A through 10K, and to GND through 10K, depop both	SI2	
75	2013/07/04	36			1. Connect J3G1.6 (WWAN_OFF_N_1) to U3F.B16 (GPIO_S5_22) through 0ohm resistor, pop 2. Depop R363	SI2	
76	2013/07/04	28			1. Pop R300 & R305 2. Depop R294 & R298	SI2	
77	2013/07/05				Reserve RC filter pad for the following signals: 1. SOC_SPI_CLK. As close to SoC side as possible, without any risk to Power Delivery Scheme 2. UIM_CLK, close to J3G1	SI2	
78	2013/07/05	34			Reserve RC delay circuit on BT_DEV_EN and WL_DEV_EN	SI2	
79	2013/07/08	35			1. Change R4623 from 24.9 +-1% 1210 to 6.04 +-1% 1210 and change from no insert to insert 2. Change value of C318 and C320 to 39pF	SI2	Omega
80	2013/07/08	34			add R436, C430 for "BT_DEV_EN" RC delay circuit	SI2	Omega
81	2013/07/09	34		RF Ross request	change net name from "BT_REG_ON" to "BT_DEV_WAKE"	SI2	Omega
82	2013/07/09	26		RF Ross request	delete JEDP2 connector	SI2	Omega
83	2013/07/09	36			Depop R350, R357, R341, R340, R424, R377	SI2	Omega
84	2013/07/10	13			Depop R95, Change C40 to R274 (0ohm resistor) and pop	SI2	Omega
85	2013/07/10	12			Separate the following PWR_RVD_V1P0 pins from +V1P0S to +VIP0S_PCIE_SATA -- BCl, BB2, BB15, BG1, BF2	SI2	Omega
86	2013/07/10	20			add R285, R359, R381, R437, R439, R442 I2C PU resistors near device side	SI2	Omega
87	2013/07/11	26			Add Q4607, Q4608, R444, R449, R450, R451 for Panel enable pin level shift	SI2	
88	2013/07/12	20			Pop PU resistors as values in the following: R3, R4, R5, R6: 1.2k	SI2	
89	2013/07/12	9			Change C8 & C9 to 27pF for RTC fine-tune	SI2	
90	2013/07/16	9			Change C8 & C9 to 22pF for S5 RTC fine-tune	SI2	
91	2013/07/16	35			Change values for NFC tuning as the following: 1. C317 & C319 = 120pF 2. C323 & C324 = 22pF 3. C316 & C321 = 120pF 4. C398 & C399 = NC	SI2	
92	2013/07/17	28			De-pop R293; pop R299	SI2	

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